Lanthanum Fluoride charge trapping layer with silicon nanocrystals for nonvolatile memory device application

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Abstract: Silicon nanocrystals (Si-NCs) embedded in a Lanthanum Fluoride (LaF_3) insulating layer were fabricated as a charge trapping layer by a simple Chemical Bath Deposition (CBD) technique. The X-Ray diffraction of the deposited layer shows a polycrystalline LaF_3 deposition on silicon. The charge storage behavior of Si-NCs embedded in the LaF_3 layer have been investigated in metal-insulator-semiconductor (MIS) structures by electrical characterization, where various interface traps and defects were introduced by thermal annealing treatment. The flat-band voltage shift of capacitance-voltage *(C–V)* and conductance-voltage *(G–V)* curves of Si: NC-MIS devices were found to exhibit charge trapping. The current-voltage *(I–V)* measurement also demonstrate that traps have strong influence on the charge storage behavior, in which the traps and defects at the internal/surface of silicon nanocrystals and the interface states at the LaF_3 /Si substrate play different roles, respectively. The flat-band voltage *(V_{FB})* shift was about 700 mV, which is agreed well enough to capture charge inside the nanoparticle for nonvolatile memory (NVM) device applications. Thickness-dependent flat-band voltage *(V_{FB})* shifts in the MIS structure which can be used as a low-voltage nonvolatile memory.

Keywords: Si Nanocrystal, MIS Devices, Nonvolatile Memory

1. Introduction

Metal-insulator-semiconductor (MIS) structures based on silicon nanocrystals or quantum dots embedded in insulator layers are widely studied for the potential applications in the field of electric devices such as single electron transistor, switching devices, memory devices [1, 2] and future very large scale integrated circuits. In recent years, researchers have been considering nanocrystal-based memory devices as a solution to ultra-large scale integration of electronic nonvolatile memories. Local defect related leakage is the major barrier to such integration for nonvolatile memory technology. This local–defect-related leakage can be reduced efficiently to improve data retention by using nanocrystals as charge storage materials instead of continuous floating gate [3]. In this regard, discrete-trap type semiconductor storage materials such as Si nanocrystals (Si-NCs) embedded in a dielectric matrix have been demonstrated as potential candidates for the fabrication of high-speed, high-density, low power-consuming, and nonvolatile memories [4-8].

Several models for charge storage mechanisms have been proposed. A possible mechanism was suggested by Tiwari *et al.* that an electron injected to the nanocrystal might fall into a trap [9].

By fabricating a charge trapping layer with large density and deep trap sites which can be used to increase the charge trapping efficiency. From this point of view, formation of Si-NCs in the charging trapping layer has been employed to enhance the charge trapping efficiency.

Metal–insulator–semiconductor (MIS) memory structures containing Si-NCs in a dielectric matrix such as silicon oxide [4, 5, 10-12] or silicon nitride [13] insulator have recently been of particular interest due to their unique properties. But very recent trend is to embed silicon nanocrystals (Si-NCs) in rare-earth halide, like Lanthanum fluoride (LaF_3), and use it in MIS devices [14].

The uses of Si-NCs-embedded Lanthanum Fluoride (LaF_3) as an insulating layer in MIS device and structural investigations on chemical-bath deposited Si-NCs-embedded LaF_3 have been reported in this article. Electrical measurements were performed using

capacitance–voltage (*C–V*), conductance-voltage *(G–V)* and current-voltage (*I–V*) technique in various annealed MIS devices having different conditions of traps. In this paper, our fabricated MIS devices that contain Si-NCs embedded in a Lanthanum Fluoride (LaF₃) charge trapping layer formed by a simple CBD process which has excellent electrical characteristics for NVM devices.

2. Experimental Details

MIS device containing a layer of Si-NCs embedded in LaF₃ insulating layer were fabricated on a p-type <111> single crystal silicon substrates. Device fabrication began with Ultrasonic cleaning of the substrate and formation of porous silicon (PS) & silicon nanocrystals (Si-NCs). Porous silicon sample were prepared by standard electrochemical etching of *p-type* <111> Si wafers in a home-made double tank cell [15] at different current densities for 30 minutes under room light illumination. Etching was done in a 2.5:1 (v/v) solution of 48% HF and absolute ethanol.

In this work, the colloidal suspensions of silicon nanocrystals were prepared from as made porous silicon in hydrofluoric (HF) acid by Ultrasonic Vibration (sonication) method at a frequency of 40 kHz [14].

After formation of the colloidal suspensions of silicon nanocrystals in HF, in the in-situ CBD technique, LaF₃ layer with embedded Si-NCs was deposited on Si by chemical reaction of LaCl₃ and the colloidal suspensions of Si-NCs in HF, and HCl solution was drained out. The samples were annealed at 100˚C and 400˚C for 10 min.

In order to the measure electrical properties of the as fabricated MIS device, 4mm² spot of silver (Ag) was coated on the both side of the prepared sample by thermal evaporation technique in using the vacuum coating (Edwards, Model: E306A) unit. The electrical and memory measurements of the Si:NC-MIS device were performed as a function of applied DC bias voltage at room temperature using an impedance analyzer (HP 4294A). The bias was swept from negative to positive and back to negative. A schematic diagram of a completed Si:NC-MIS device is shown in Fig. 1.
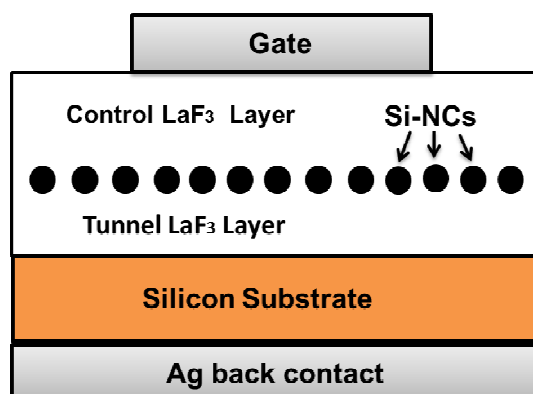

Figure 1. *Schematic diagram of a fabricated MIS structure.*

3. Results and Discussion

The structural analysis of LaF₃ deposited sample was carried out using X-ray diffractometer varying diffraction angle 2θ from 20° to 80°. Figure 2 shows the XRD patterns of the LaF₃ deposited sample.

The diffraction peaks were observed around 2θ= 24.5°, 27.6°, 38.4°, 43.6°,50.8°, 70.7° correspond to (110), (111), (210), (300), (220) and (322) crystal orientation, respectively. The presence of a number of peaks in pattern confirms that the LaF₃ was polycrystalline nature of the material.
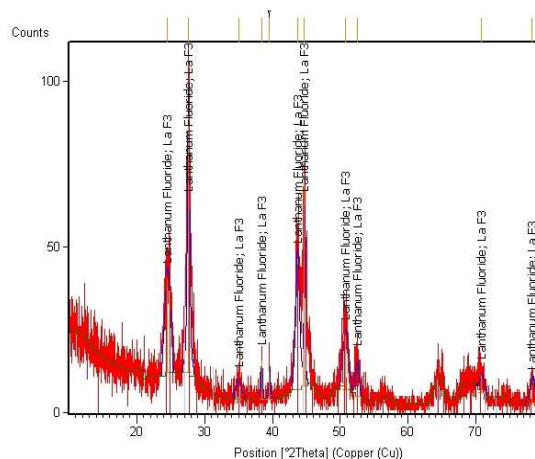

Figure 2. *XRD spectra of LaF₃ deposited sample at room temperature.*

The shift in current–voltage (I–V) characteristics at a gate 4mm² area in the MIS memory devices is shown in Fig. 3. I–V hysteresis measurement was performed from negative voltage to positive voltage (forward sweep) and vice versa (reverse sweep).
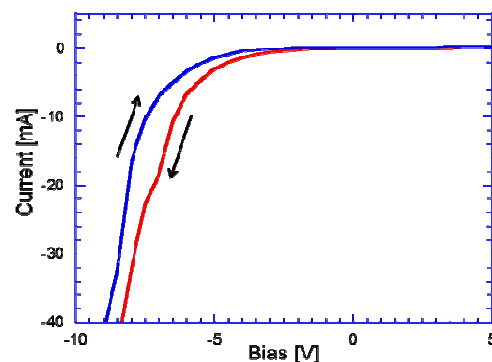

Figure 3. *Shift of I–V curve for different program/erase voltage at a gate of 4mm².*

Fig. 3 demonstrates the possible of electron trapping with a negative induced charge during program mode, and during erase mode, electron detrapping and hole trapping formed a positive induced charge. Consequently, the shift of voltage corresponds with the amount of trapped electrons. Hence, the voltage shift measured in the I–V characteristics after the biasing program voltage, i.e., the amount of trapped electrons.

Figure 4 shows the capacitance-voltage *(C–V)* hysteresis loops in various annealed MIS [Ag/LaF$_3$/Si-NCs/Si/Ag] structures based on silicon nanocrystals, where charges are stored in a nanocrystal for all samples. The *C–V* measurements were performed over a voltage range -4V to 4V and back to -4V. Small flat-band voltage *(V$_{FB}$)* shift is observed in the lower annealed MIS device as shown in Fig. 4(a). This indicates that injected charges are stored mainly in nanocrystals or at their interfaces. Maximum shift in the *C–V* hysteresis loop is obtained at 400˚C annealed device (in Fig. 4(b)) having the highest trap density, the small shift is observed in the lower annealed samples having the lowest trap density. It means that more charges are stored in the higher annealed nanocrystal than in the lower annealed one (in Fig. 5).
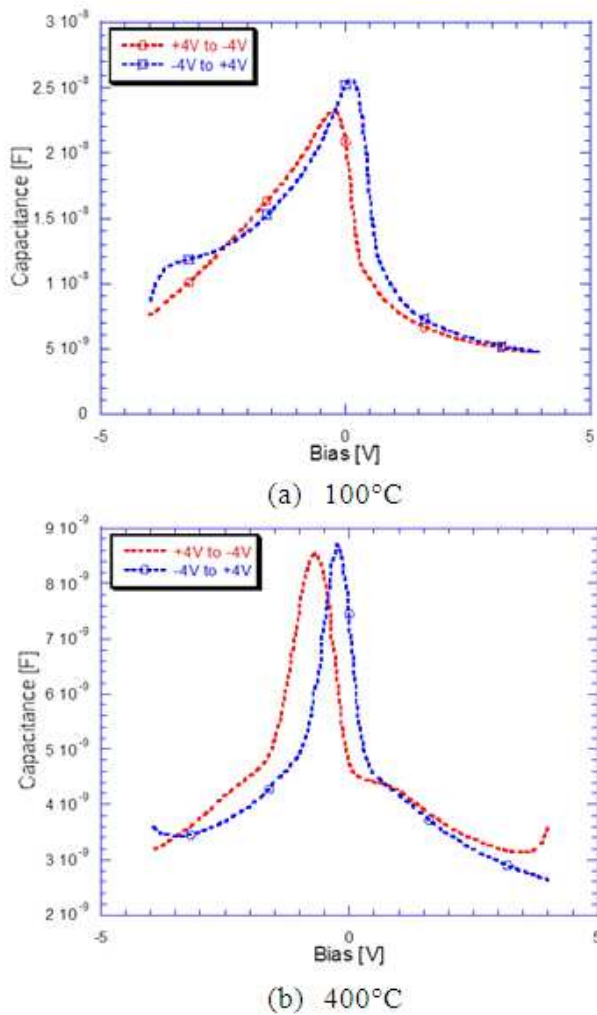

Figure 4. *Capacitance–voltage (C–V) hysteresis curve of fabricated MIS devices containing Si-NCs embedded in a LaF$_3$ layer as a charge trapping layer.*

As one can be seen from Fig.4 (a), the lower annealed MIS structure exhibit slow traps at the insulator/semiconductor interface, i.e., defects that are distributed away from the interface to the insulator. This direct tunneling of electrons from the traps to the interface states at LaF$_3$/Si substrate will produce long-term loss of trapped electrons. Evidently,

the decrease in the interface states would consequently reduce the charge-loss rate at higher temperature. Figure 5 shows the variations of capacitance peak with annealing temperature. Lower peak and enhanced peak were observed for lower annealing temperature (100°C) and higher annealing temperature (400°C), respectively, for the same annealing time. From this figure, annealing can improve the size uniformity of the Si-NCs. At the higher temperature, the size of the Si-NCs becomes more uniform than that at the lower temperature.

It is important to note that the traps and defects at the internal/surface of nanocrystals and the interface states at the LaF$_3$/Si substrate play different roles in the charge-loss process, respectively. Smaller number of the interface states would effectively result in longer retention time. Therefore, the number of trapped electrons is dominantly related to the number of deep traps, and larger *V$_{FB}$* shift could be achieved by nanocrystals with more deep traps.

The *C–V* characteristic for MIS structure clearly shows a hysteresis loop which indicates net charge trapping in the MIS capacitor. The presence of such sites is attributed to the quantum-confinement effect of the silicon nanocrystals. Due to variations of applied voltage from accumulation and depletion, the flat-band voltage shift of the *C–V* curve is approximately 700 mV, which is enough to capture charge inside the nanoparticle.
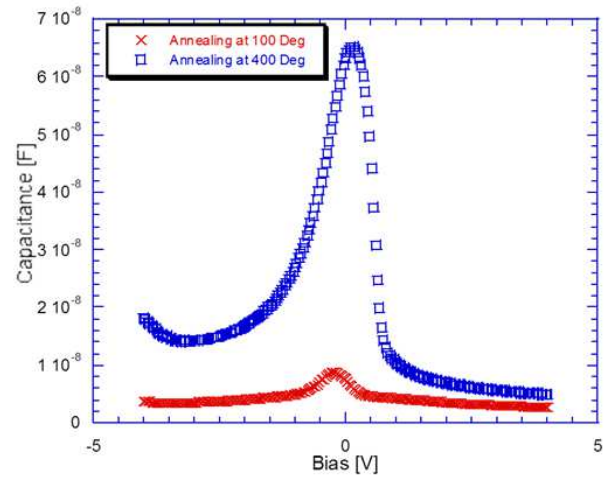

Figure 5: *Annealing effect on C-V measurements.*

The charging characteristic occurs by tunneling process of the Si NCs in thickness dependent *C-V* measurements, as shown in Fig. 6. From Fig. 6 it can be shown that a memory window of about 50 mV to 500 mV is achievable at a bias voltage of (-2V to +2V) and about 500 mV to 1036 mV is achievable at a bias voltage of (-4V to +4V). It is seen that at a different bias voltage for different insulating layer thickness a smaller range flat-band voltage shift for the first one, and for the latter case, it is a larger flat-band voltage shift(in Fig. 6). So a significant memory window (700 mV) has been achieved over a small bias voltage (-4V to +4V) at 75nm layer thickness, which indicates this type of MIS structure used as a low voltage nonvolatile memory device.
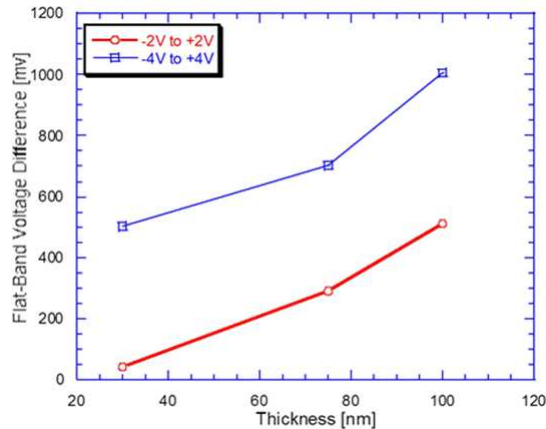
Figure 6: *Flat-band (VFB) shift difference versus different charge trapping layer thickness.*

Figure 7 shows the *G–V* curve for the Ag/LaF₃/Si-NCs/Si/Ag structure. In the figure, the presence of conductance peak with a peak position close to the flat-band voltage around the *C–V* flat-band voltage in both the forward and the reverse *G-V* measurements.
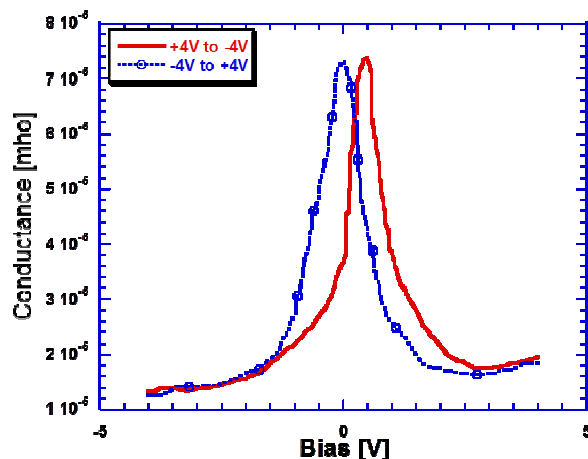

Figure 7. *Shift in conductance-voltage (G–V) peak position curve of LaF₃ with Si-NCs for different program/erase voltage.*

The conductance-voltage (*G–V*) study also revealed that the same hysteresis as like *C–V* characteristics. The magnitude of the hysteresis in *C–V* and the shift in the peak position in *G–V* are both about 0.7V.

Electron trapping and de-trapping were observed in the conductance peak. Therefore, these hysteresis and peak shifts could be attributed to electrons trapped in silicon nanocrystals in LaF₃ insulating layer. This result indicates that the Ag/LaF₃/Si-NCs/Si/Ag structure can be used as a floating gate in nonvolatile single electron memory devices.

4. Conclusions

In summary, the charge storage characteristics in the MIS memory structures based Si-NCs embedding in LaF₃ as an alternative charge trapping layer have been investigated successfully. It was observed in X-ray diffraction (XRD) spectra that the deposited LaF₃ layer was polycrystalline in nature. By studying the electrical characteristics of the fabricated lanthanum fluoride charge trapping layer with silicon nanocrystals for MIS devices, we observed carrier exchange were possible between the semiconductor substrate and bound states quantum confinement of carriers in the NCs

Based on the *C-V* and *G-V* experimental evidence, the charge storage characteristics have been demonstrated. *C-V* hysteresis curves were obtained with increasing sweep bias range, indicating the electron injection from the substrate to the charge trapping layer. By introducing a certain number of deep trapping centers in nanocrystals and decreasing the interface states at LaF₃/Si substrate, large memory window can be achieved. It was also observed charge trapping mechanism in current–voltage *(I–V)* measurement. The present results suggest that Si-NCs embedded in a LaF₃ trapping layer hold good promise for potential applications in low voltage nonvolatile memories.

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