



Security of Hardware Architecture, Design and Performance of Low Drop-Out Voltage Regulator LDO to Protect Power Mobile Applications

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Abstract: His paper present a new Low Drop-Out Voltage Regulator (LDO) and highlight the topologies and the advantages of the LDO for hardware security protection of Wireless Sensor Networks (WSNs), this integrated circuits are considered as an ideal solution in low power System on-chip applications (SOC) for their compact sizes and low cost. The advancement in low-power design makes it possible that ubiquitous device can be powered by low-power energy source such as ambient energy or small size batteries. In many well supplied devices the problem related to power is essentially related to cost. However for low-powered devices the problem of power is not only economics but also becomes very essential in terms of functionality. Due to the usual very small amount of energy or unstable energy available the way the engineer manages power becomes a key point in this area. Therefore, another focus of this dissertation is to try finding ways to improve the security of power management problems. Complementary metal oxide-semiconductor (CMOS) has become the predominant technology in integrated circuit design due to its high density, power savings and low manufacturing costs. The whole integrated circuit industry will still continue to benefit from the geometric downsizing that comes with every new generation of semiconductor manufacturing processes. Therefore, only several CMOS analog integrated circuit design techniques are proposed for low-powered ubiquitous device in this dissertation. This paper reviews the basics of LDO regulators and discusses the technology advances in the latest generation of LDOs that make them the preferred solution for many points of load power requirements. The paper will also introduce characteristics of CMOS LDO regulators and discuss their unique benefits in portable electronics applications. these new device offer a real advantages for the power management security of new applications mobile. Power efficiency and some practical issues for the CMOS implementation of these LDO structures are discussed.

Keywords: Security, LDO, WSNs, Low Power SOC, Integrated Circuit, CMOS Low-Power

1. Introduction

In the modern technology, the security of hardware power management has become an increasingly important design consideration for numerous products, especially those relying on battery power. Complicating the power management situation, as more features get integrated into hardware products, the number of required voltage supplies increases. between 3.6V-5.5V lithium-ion battery, a highly integrated product such as a smart phone, WSN can require more than ten different voltages such us Global positioning system,

Audio Power amplifier [13-22], Memory, Baseband and DSP core, Applications (picture, music and video) processing, Low voltage wireless Sensor Networks and LAN, Display back light drivers, Photo flash charger To handle all of these voltages [23-40], one of the main contributions also is an elaborate power simulation with any level of accuracy which can still be balanced with complexity.

The simulated power consumption in System On Chip (SOC) can depend on the supply voltage, for example, for a nearly empty battery when supplying a microcontroller that operates at very low voltages. In WSN nodes, components

with different supply voltages are combined resulting in the need for LDOs [1-6] and DC/DC converters [7-12]. The Power Aware Wireless Sensor framework PAWiS allows modeling this hierarchical supply structure as well as the efficiency factor of the converters.

The PAWiS framework is based on the OMNeT++ discrete event simulator and the C++ programming language. Figure 1 depicts the structure of the framework from the users view. The model programmer mostly interacts with the framework

and C++. Additionally basic knowledge of concepts of OMNeT is required to comprehend the simulation process.

The node compositions as well as the network layout are specified in configuration files. Completed models can be compiled (optionally with a GUI based on Tcl/Tk) to an executable simulator. With the optional GUI the workflow and communication of the model can be observed during the simulation. Additionally a log file with power and timing profile is generated for post-simulation analysis.

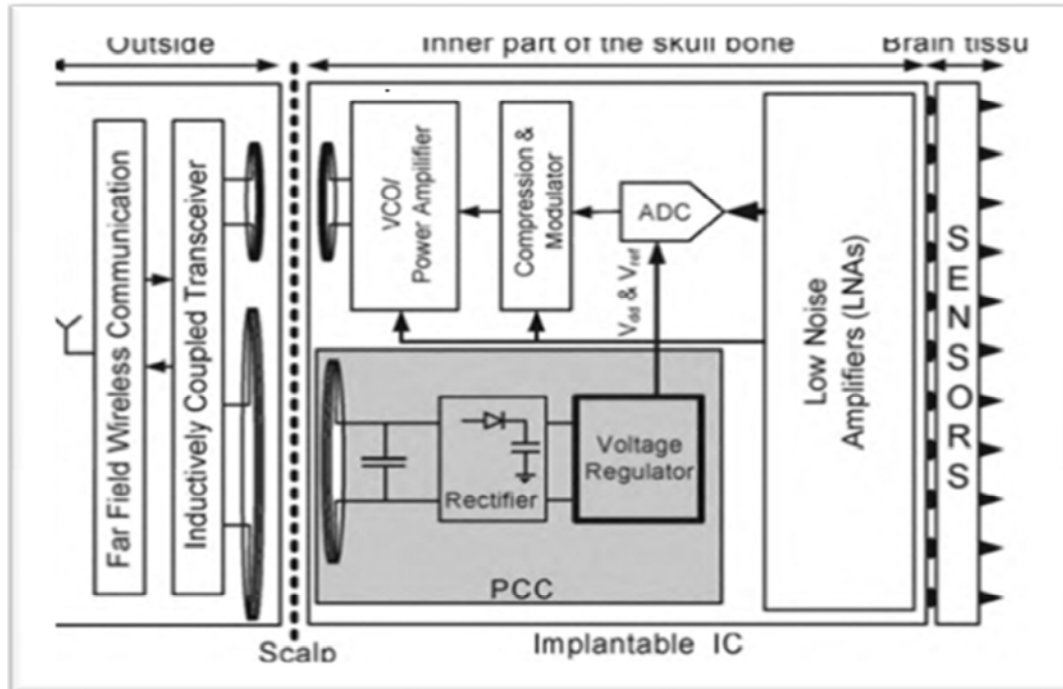


Figure 1. Regulator integrated in the SOC.

This paper reviews the most important element in the hardware blocs, LDO, dedicated to protect and provide a secure and stable power alimentation and discusses the technology advances in the latest generation of LDOs that

make them the preferred solution for many points of load power requirements. The paper will also introduce the characteristics of CMOS LDO regulators and discuss their unique benefits in mobile electronics applications.

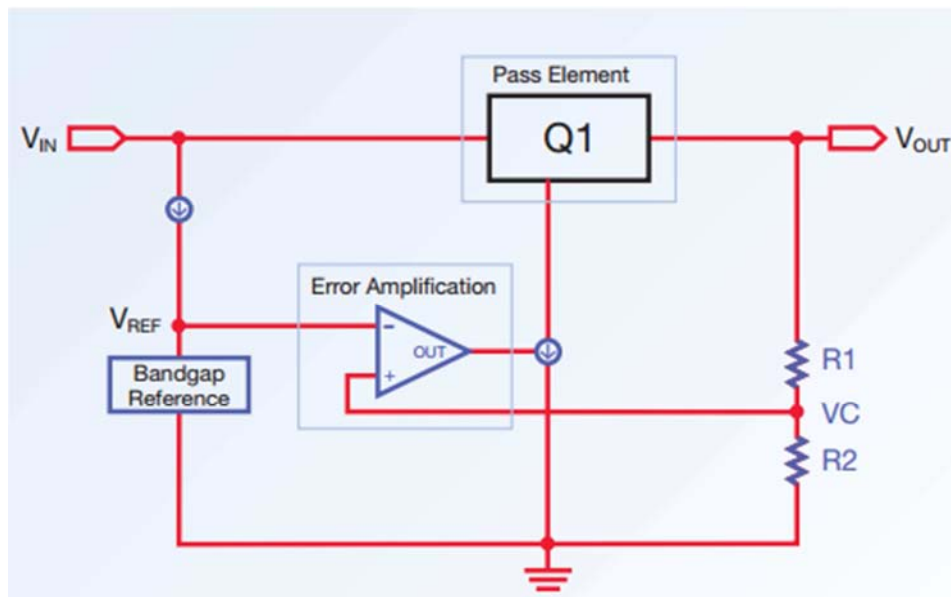


Figure 2. The Q1 in LDO can be a Darlington pair, or an N-channel or P-channel MOSFET.

2. Pmos-Type Regulators: Studies and Simulations

An MOS-type LDO regulator is shown in figure 2. It is composed of three main parts:

- Power transistor (Pass Element)
- Error amplification
- Resistance reaction (R1, R2).

3. Output Voltage

The power transistor is used as a current source controlled by the error amplifier. V_0 at the output of the divider bridge (R1, R2) is compared with the reference voltage V_{ref} . The output voltage is given by:

$$V_o = V_{ref} \left(1 + \frac{R1}{R2}\right) \quad (1)$$

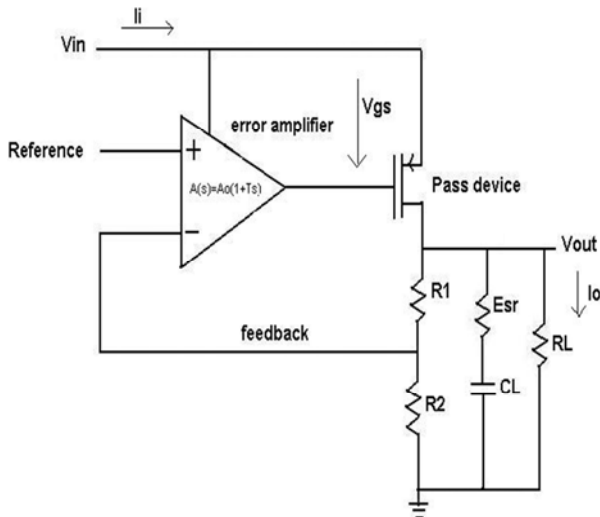


Figure 3. Diagram of a Linear Regulator LDO.

3. Efficiency

The efficiency of a regulator is defined by the equation:

$$Efficiency = \frac{V_o \cdot I_o}{V_i \cdot (I_o + I_q)} * 100 \quad (2)$$

Where I_q is the quiescent current of the regulator.

When I_q is negligible before equation (2) becomes:

$$Efficiency = \frac{V_o}{V_i} * 100 = \frac{V_i}{V_i} * 100 = \left(\frac{V_{ds}}{V_i} + 1 \right) * 100 \quad (3)$$

Where V_{ds} is the drain-source voltage of the power transistor. The efficiency of an LDO controller depends on the voltage across the power transistor.

4. DC Load-Regulation

The Load-Regulation DC (DC-LOR) is the difference between the maximum and the minimum of the output voltage V_{OUT} , when I_{LOAD} varies from 0mA to 50mA.

In other words, it defines the output impedance of the controller:

$$Z_{out} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \quad (4)$$

The DC Load regulation represents the ability of the system to adjust the variation of the output voltage. It is given by:

$$\frac{\Delta V_o}{\Delta I_o} = \frac{1}{g_{mp} \cdot A_o} * \frac{R1 + R2}{R2} \quad (5)$$

Consequently, a small change in the output current (FIG. 6) corresponds to it a voltage variation of the power transistor MP:

$$\Delta V_{gsMP} = \frac{\Delta I_o}{g_{mp}} \quad (6)$$

Which corresponds to the variation of the input of the amplifier:

$$\Delta V_A = \frac{\Delta V_{gsMP}}{A_o} = \frac{\Delta I_o}{g_{mp} A_o} \quad (7)$$

Furthermore:

$$\Delta V_A * \frac{R1 + R2}{R2} = \frac{\Delta I_o}{g_{mp} \cdot A_o} * \frac{R1 + R2}{R2} \quad (8)$$

Thus we can deduce the DC-LOR:

$$\frac{\Delta V_o}{\Delta I_o} = \frac{1}{g_{mp} \cdot A_o} * \frac{R1 + R2}{R2} \quad (9)$$

Or:

a. g_{mp} is the DC transconductance of the power transistor

b. A_o the DC gain of the error amplifier.

Note that the DC-LOR is limited by the open-loop gain.

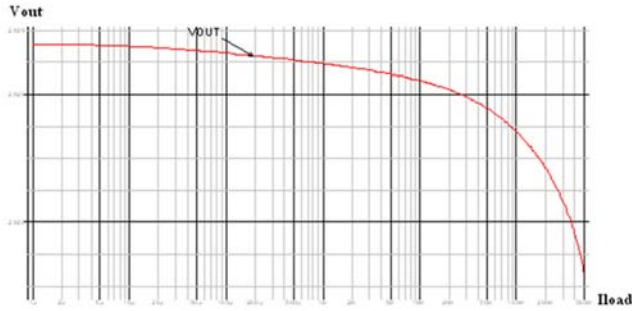


Figure 4. *Vout vs Iload.*

5. DC Line-Regulation

The DC Line-Regulation (DC-LIR) is defined as the difference between the maximum and the minimum of the output voltage V_{OUT} , when V_{IN} varies from 3.0V to 5.5V

The typical value of V_{OUT} (V_{OUT_REG}) is defined when $V_{IN} = 3.6V$.

The dropout at 100mV is the value of the voltage difference ($V_{IN} - V_{OUT}$) when $V_{IN} = V_{OUT_REG} - 100mV$, defined for $I_{LOAD} = 50mA$

The DC-LIR is the ability of the system to maintain the output voltage stable. This DC-LIR is given by:

$$line\ Regulation = \frac{\Delta V_o}{\Delta V_i} = \frac{\Delta V_o}{\Delta I_o} \cdot \frac{\Delta I_o}{\Delta V_i} \quad (10)$$

After development, we obtain:

$$line\ Regulation = \frac{1}{g_{mp} \cdot A_o} * \frac{R1 + R2}{R2} * \frac{1}{(R_{ds} + R_L)} \quad (11)$$

Where R_{ds} is the equivalent resistance of the power transistor.

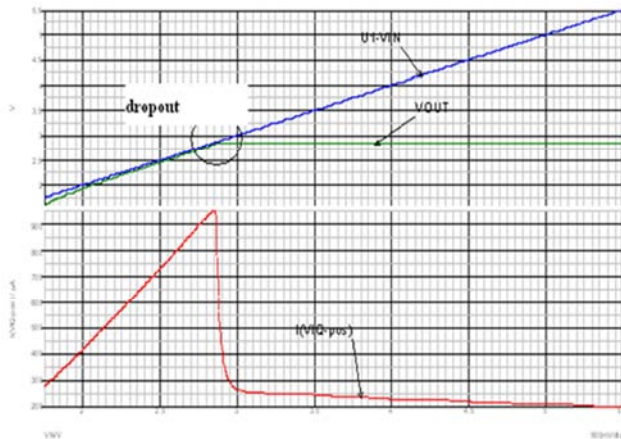


Figure 5. *Analyse DC Vout vs Vin.*

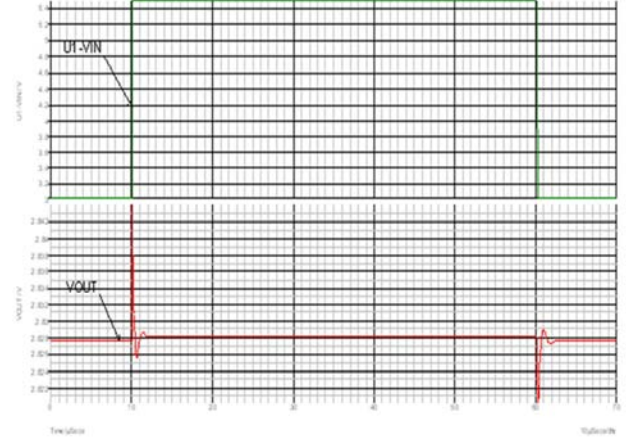


Figure 6. *Transient variation of Output voltage as a function of the input voltage.*

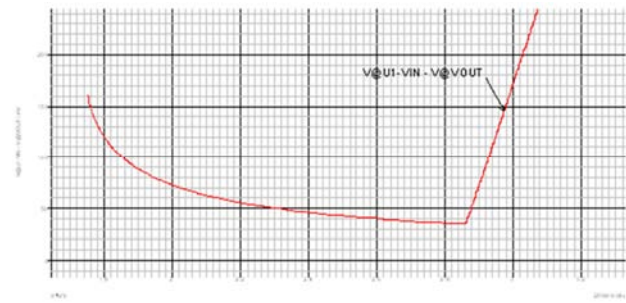


Figure 7. *Zoom of output voltage.*

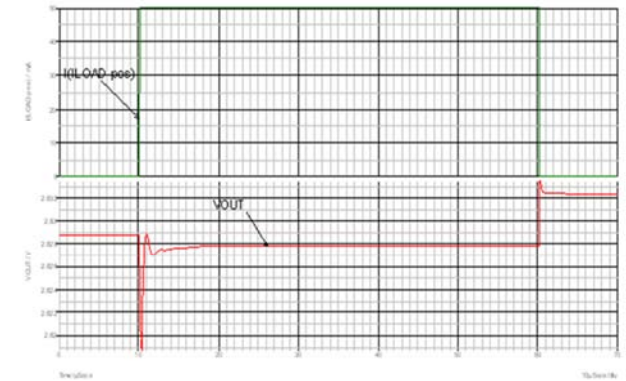


Figure 8. *Transient variation of the output voltage as a function of the load current of the LDO controller.*

6. AC Line-Regulation

This simulation consists in varying in time (transient simulation) V_{IN} , and measuring the behavior in time of V_{OUT} .

The AC-LIR dynamic line control is the peak-to-peak difference of V_{out}

The number of bounce in the curve is directly related to the stability of the I_{do}

7. AC Load-Regulation

The AC-load regulation AC-LOR is the peak-to-peak difference of V_{out} .

This simulation consists in varying in time (transient simulation) ILOAD and measuring the behavior in time of V_{OUT} . With fixed V_{IN} .

8. PSRR

The PSRR is the frequency gain between V_{in} (f) and V_{out} (f). We will compute this PSRR of the regulator given in figure 9.

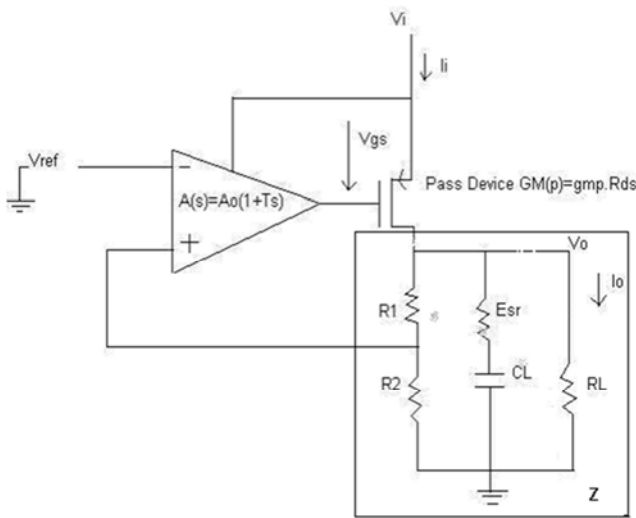


Figure 9. Régulateur LDO.

We have:

$$V_o(s) = -g_m Z V_{gs}(s) \quad (12)$$

with

$$Z = R_L // (R_1 + R_2) // \left(E_{SR} + \frac{1}{C_L S} \right) = \frac{R_S (1 + E_{SR} C_L S)}{1 + (E_{SR} + R_S) C_L S}$$

$$(R_S = R_L // (R_1 + R_2))$$

$$V_o(s) = -g_m Z \left(\frac{A(s) V_o(s) R_2}{R_1 + R_2} - V_i(s) \right) \quad (13)$$

$$PSRR(s) = \frac{V_o(s)}{V_i(s)} = \frac{g_m Z}{1 + g_m Z \frac{R_2}{R_1 + R_2} A(s)} \quad (14)$$

Or $A(s)$ and the gain of the error amplifier given by

$$A(s) = \frac{A_0}{1 + T s}$$

Particular case:

To simplify the calculations we will take $ESR = 0$.

By developing equation (14) we obtain:

$$PSRR(s) = \frac{g_m R_S (R_1 + R_2) (1 + T s)}{R_1 + R_2 + g_m R_S R_2 A_0 + s((R_1 + R_2) T + R_S C_L (R_1 + R_2)^2 R_S C_L T (R_1 + R_2))} \quad (15)$$

The equation shows that the system has a zero and two real or complex poles depending on the behavior of several parameters:

if $g_m R_S R_2 A_0 \gg R_1 + R_2$ et $R_S C_L \gg T$, equation (14) becomes:

$$PSRR = \frac{g_m R_S (R_1 + R_2) (1 + T s)}{g_m R_S R_2 A_0 + s R_S C_L (R_1 + R_2) + s^2 R_S C_L T (R_1 + R_2)} \quad (16)$$

$$PSRR = \frac{(R_1 + R_2) (1 + T s)}{R_2 A_0 + \left(1 + s \frac{C_L (R_1 + R_2)}{g_m R_2 A_0} + s^2 \frac{C_L T (R_1 + R_2)}{g_m R_2 A_0} \right)} \quad (17)$$

The equation 17 the form of:

$$PSRR(s) = \frac{(R_1 + R_2) (1 + T s)}{R_2 A_0} \frac{1}{1 + s \frac{1}{\omega_o Q} + s^2 \frac{1}{\omega_o^2}} \quad (18)$$

with:

$$\omega_o = \sqrt{\frac{g_m R_2 A_0}{(R_1 + R_2) C_L T}}$$

$$Q = \sqrt{\frac{g_m R_2 A_0 T}{(R_1 + R_2) C_L}}$$

The equation: $\frac{1}{1 + s \frac{1}{\omega_o Q} + s^2 \frac{1}{\omega_o^2}}$ Shows the existence of

two real or imaginary poles:

Real Poles:

Got it!

$$Q < \frac{1}{2} \Leftrightarrow \frac{g_m}{C_L} < \frac{R_1 + R_2}{R_2} * \frac{1}{4 A_0 T} \Leftrightarrow \frac{1}{T} > \frac{4 A_0 R_2}{R_1 + R_2} * \frac{g_m}{C_L} \quad (19)$$

In this case the PSRR becomes:

$$PSRR(s) = \frac{(R_1 + R_2) (1 + T s)}{R_2 A_0} \cdot \frac{1}{(1 + T s) \left(1 + \frac{(R_1 + R_2) C_L}{g_m R_2 A_0} s \right)} \quad (20)$$

$$= \frac{R_1 + R_2}{R_2 A_0} \cdot \frac{1}{1 + \frac{(R_1 + R_2) C_L}{g_m R_2 A_0} s}$$

Real or complex pole:

$$\text{when } Q > \frac{1}{2} \Leftrightarrow \frac{g_m}{C_L} > \frac{R_1 + R_2}{R_2} * \frac{1}{4 A_0 T} \Leftrightarrow \frac{1}{T} < \frac{4 A_0 R_2}{R_1 + R_2} * \frac{g_m}{C_L}$$

$$\text{In this condition: } \frac{1}{1 + s \frac{1}{\omega_o Q} + s^2 \frac{1}{\omega_o^2}}$$

Has a peak of amplitude at the frequency:

$$f_p = \sqrt{\frac{1}{8\pi^2 T^2} \left(\frac{2A_o}{R1 + R2} \right) \cdot \frac{gm}{CL} \cdot T - 1} \quad (21)$$

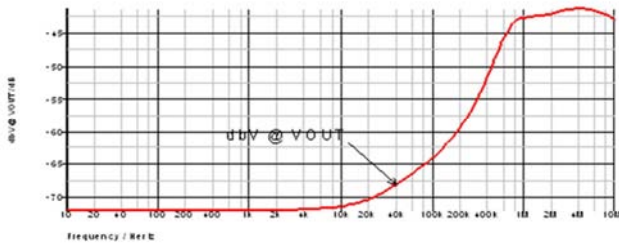


Figure 10. Le PSRR of LDO.

9. Conclusion and Perspectives

In this paper we proposed a new structure corresponding to a pmos type ldo. By this work, we improved the stability and security of our regulator by adding a doublet (zero, pole).

The expression relating to the different poles was elaborated. The latter have shown the dependence of the stability of the load current.

The simulations studied thus confirmed this result. in order to remedy this problem, it is necessary to try to design a new structure whose stability is independent of the load current.

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