

# Scrutiny of Leakage Currents with Insulating Materials for Transistor Applications

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**Abstract:** Continuous reducing the size of transistor technology has enabled extraordinary improvements in the switching speed, density, functionality and cost of microprocessors. Integrated Circuit industry is pursuing Moore's curve down to deep-nanoscale dimensions. Advanced transistor technology now faces many challenges that together result in static power consumption due to leakage currents. In fact, leakage currents are responsible for more than 50% of the total power consumption in nanoscale designs. In deep-nanoscale arena, this percentage will increase further. However, diagnosing of the interface quality and interaction between insulators and semiconductors is significant to reduce the leakage current and achieve the high performance of switching devices in the nanoscale domain. Continuous scaling down has required drastic decreases of the SiO<sub>2</sub> dielectric film thickness to achieve ever-higher capacitance densities. Fundamental limits of SiO<sub>2</sub> as a dielectric material, imposed by electron tunneling, will be reached as this SiO<sub>2</sub> film thickness approaches ~1nm. Therefore, alternate high-k interlayer dielectric material will be needed to replace SiO<sub>2</sub> as a capacitor and gate dielectric material. Numerous alternate high-k materials are being actively investigated, ranging from Al<sub>2</sub>O<sub>3</sub> (k ~ 9) to HfO<sub>2</sub> (k ~ 25). High-k materials hold the promise of achieving very high capacitance densities with relatively thick films.

**Keywords:** Dielectric Materials, High-k Materials, Hafnium Oxide, MOS Transistor, Nanoscale Domain

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## 1. Introduction

The semiconductor microelectronics and nanoelectronics industry requires interlayer dielectric films for a variety of applications [1]. Dielectric layers are needed as gates in 2-D nanostructures, graphene, hexagonal boron nitride (h-BN), and more recently the rich family of transition metal dichalcogenides (TMDs) comprising molybdenum disulphide (MoS<sub>2</sub>), WS<sub>2</sub>, WSe<sub>2</sub>, as capacitors to store charge in memory devices, and as insulation in back-end interconnects [2-3]. Silicon dioxide (SiO<sub>2</sub>) has been the dielectric material of choice for all of these applications. Silicon dioxide (SiO<sub>2</sub>) is a dielectric material with very low leakage currents, acts as a good diffusion barrier for dopants and ionic contaminants, and forms a well-defined interface with silicon. The continued drive towards faster processors has required the progressive shrinking from microelectronics to

nanoelectronics devices [1]. The decrease in device feature size allows for increased speed, lower power consumption, and lower cost because of the increased density of devices per wafer. This size reduction presents challenges for the various SiO<sub>2</sub> applications. The insulation of interconnects requires lower dielectric constant materials. Applications such as capacitors and gate dielectrics require higher dielectric constant materials. Decreasing the thickness of the SiO<sub>2</sub> dielectric film achieves the goal of increasing the capacitance to offset the decrease in the surface area of the capacitor. However, SiO<sub>2</sub> films will soon need to be so thin that tunneling through the film will become significant and will increase power consumption to unacceptable levels. High-k materials are needed to replace SiO<sub>2</sub> in these applications to achieve high capacitances while keeping the leakage currents low [4-5].

As devices approach the sub-45 nm scale, the effective oxide thickness (EOT) of the traditional silicon dioxide

dielectrics are required to be smaller than 1 nm, which is approximately three (3) monolayers and close to the physical limit, thus resulting in high gate leakage currents due to the obvious quantum tunneling effect at this scale [25]. To continue the downward scaling, dielectrics with a higher dielectric constant (high-k) are being suggested as a solution to achieve the same transistor performance while maintaining a relatively thick physical thickness. Many candidates of possible high-k gate dielectrics have been suggested to replace  $\text{SiO}_2$  and they include nitride  $\text{Si}_3\text{N}_4$ , Hf-based oxides, and Zr-based oxides. Hf-based oxides have been recently highlighted as the most suitable dielectric materials because of their comprehensive performance in order to continue manufacturing low-cost semiconductor products, its dimension and concentration, like oxide thickness and substrate profile and device structure [6-7, 28].

The rest of this paper is organized as follows. Section II discuss about the requirement for transistors in the context of memory and gate applications. Various emerging dielectric materials are discussed in Section III. Section IV shows the effect of insulating materials on leakage currents. Finally, a summary and conclusion is drawn by Section V.

## 2. Requirements for Memory and Gate Applications

Memory capacitor and gate applications both need alternate high-k dielectrics to achieve higher capacitance densities [27]. However, the requirements for memory capacitor and gate applications are different [1]. Capacitors for memory need very low leakage currents density on the order of  $10^{-8}$  A/cm<sup>2</sup>. This requirement allows the charge stored in the capacitor to remain large enough to be read for a relatively long time period, typically ~250 ms [18]. In contrast, the nature of the high-k/electrode interface is not that critical, provided that the interface does not reduce the capacitance significantly. Metal or highly doped nitrided poly-Si may be used as the electrodes. High-k dielectrics grown by atomic layer deposition. Gate dielectrics in FETs can have a much higher leakage current, but the quality of the high-k/Si bottom electrode interfacial region is critical [1]. Current densities as high as 1–10 A/cm<sup>2</sup> are acceptable for some processors. Certain low power applications, such as portable devices, demand leakage currents of  $< 10^{-3}$  A/cm<sup>2</sup>. These leakage current levels are still much less stringent than the requirements for memory capacitors. More important to the performance of an FET is the electric field that penetrates into the silicon channel. Interfacial layers and interface roughness adversely affect the strength and uniformity of this electric field and degrade FET performance [1].

## 3. High-k Dielectric Materials

Most of the known binary metal oxide high-k materials have been grown by ALD. These binary metal oxide materials include, approximately in order of increasing

dielectric constant,  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ , and  $\text{TiO}_2$ . The dielectric constants of these thin films grown by ALD range from  $k \sim 10$  to  $k \sim 100$ . These dielectric constants are comparable with the dielectric constants measured for the same materials grown by other methods. In this section, a literature survey on five oxide material are given and a comparative study is shown in Table 1.

### 3.1. Titanium Oxide ( $\text{TiO}_2$ )

$\text{TiO}_2$  ALD film growth has been described in numerous papers [4, 30]. However, no dielectric constant values have been reported in these studies. Previous researchers have indicated that their  $\text{TiO}_2$  ALD films were too leaky to measure the dielectric constant [5]. Titanium precursors included  $\text{TiCl}_4$ ,  $\text{TiI}_4$ ,  $\text{Ti}(\text{OCH}(\text{CH}_3)_2)_4$ , and  $\text{Ti}(\text{OC}_2\text{H}_5)_4$  [4].  $\text{H}_2\text{O}$  and sometimes  $\text{H}_2\text{O}_2$  are used as the oxygen precursor. Dielectric constant values for  $\text{TiO}_2$  include  $k = 50$  [3],  $k = 80$  [1] and  $k = 100$  [2] depending on the crystalline phase of the  $\text{TiO}_2$ .

### 3.2. Aluminium Oxide ( $\text{Al}_2\text{O}_3$ )

Alumina is the more common name of Aluminium Oxide ( $\text{Al}_2\text{O}_3$ ) and is a hard wearing material used for many applications. Once fired and sintered, it can only be machined using diamond-grinding methods. Aluminium oxide is an electrical insulator but has a relatively high thermal conductivity (40 W/m K). In its most commonly occurring crystalline form, called corundum, its hardness makes it suitable for use as an abrasive and as a component in cutting tools. Aluminium oxide is responsible for metallic aluminium's resistance to weathering. Metallic aluminium is very reactive with atmospheric oxygen, and a thin passivation layer of alumina quickly forms on any exposed aluminium surface. This layer protects the metal from further oxidation. The thickness and properties of this oxide layer can be enhanced using a process called anodising. A number of alloys, such as aluminium bronzes, exploit this property by including a proportion of aluminium in the alloy to enhance corrosion resistance. The alumina generated by anodising is typically amorphous, but discharge assisted oxidation processes such as plasma electrolytic oxidation result in a significant proportion of crystalline alumina in the coating, enhancing its hardness.

### 3.3. Silicon Nitride ( $\text{Si}_3\text{N}_4$ )

Silicon nitride-based ceramics have many excellent properties, high strength and relatively high fracture toughness, good wear resistance, good oxidation resistance and good corrosion resistance. For some time, they have been under consideration as high-performance structural materials because of their superior thermal shock resistance relative to oxide ceramics [8]. Silicon Nitride has been densified with sintering additives because of the highly covalent Si-N bonding. After sintering, these additives remain as the amorphous grain boundary phase, which severely deteriorates the high-temperature mechanical behavior of

Silicon Nitride ceramics [9]. Dielectric films of silicon nitride ceramics play an integral role in nearly every semiconductor device and integrated circuit. Among this Silicon Nitride ceramic is used as a gate dielectric layer, diffusion barrier and optoelectronic-integrated circuits [10]. Low-density porous silicon nitride [11] ceramic is an important material with properties including low dielectric constant, good mechanical, high resistance to rain erosion and sand erosion. Hence, low-density porous silicon nitride ceramic is also a candidate for application in radome materials. Microstructural control of the interface and interlayer requires a complex interplay between initial composition and post-heating transformations. Nowadays most silicon nitride ceramics are prepared using  $\alpha$ - $\text{Si}_3\text{N}_4$  powders. In silicon nitride ceramics, the microstructure is similar to whisker-reinforced ceramic composites, with large rod like  $\beta$ - $\text{Si}_3\text{N}_4$  grains as the reinforcing agents [12].

### 3.4. Zirconium Oxide ( $\text{ZrO}_2$ )

Zirconium oxide ( $\text{ZrO}_2$ ) has attracted much attention as a high-K material because of its high temperature stability and high mechanical strength [13]. Thin films of  $\text{ZrO}_2$  can be prepared by many methods like sol-gel, spin coating, ALD, reactive sputtering, MOCVD, E-beam evaporation, pulse laser ablation, and rapid thermal CVD [14]. Unfortunately, oxides of zirconium ( $\text{ZrO}_2$ ) tend to crystallize much more rapidly than  $\text{SiO}_2$ , which makes the interface surface rough. So the key issue will be to form amorphous oxides of the metal initially, which might transform into the crystalline state during thermal cycling. One current avenue of investigation is to incorporate silicon (Si), Al, or N<sub>2</sub> into the random network structure [15]. Indeed, adopting the above theory, zircon ( $\text{ZrSiO}_4$ ), a compound of  $\text{ZrO}_2$  and  $\text{SiO}_2$ , has shown better interface behavior with silicon (due to its dangling bonds) and has provided more symmetric band alignment with much higher conduction band offsets compared to  $\text{ZrO}_2$  (2.10 eV compared to 0.64–1.2 eV of  $\text{ZrO}_2$ ).

### 3.5. Hafnium Oxide ( $\text{HfO}_2$ )

Among the various requirements of gate dielectric

materials, the most important are good insulating properties and capacitance performance. Because the gate dielectric materials constitute the interlayer in the gate stacks, they should also have the ability to prevent diffusion of dopants such as boron and phosphorus and have few electrical defects which often compromise the breakdown performance. Meanwhile, they must have good thermal stability, high recrystallization temperature, sound interface qualities. With regard to capacitance performance, the requirement is that the k value should be over 12, preferably 25–30. An appropriate k value means that the dielectrics will have a reasonable physical thickness which is enough to prevent gate leakage and not too thick to hamper physical scaling when achieving the target EOT. CVD and ALD deposited oxides ( $\text{HfO}_2$ ), silicates ( $\text{HfSiO}_x$  and  $\text{HfSiON}$ ) and aluminates of hafnium (Hf) show higher k and lower leakage current than  $\text{SiO}_2$  at the same EOT. The materials also offer a higher limiting offset barrier (0.5 eV) [16] besides being stable thermodynamically and electrically over silicon (Si) at high temperatures [17]. At the same time silicon dioxide and oxynitride, the traditional gate dielectric materials in field effect transistors (FETs), are rapidly approaching their ultimate thickness.

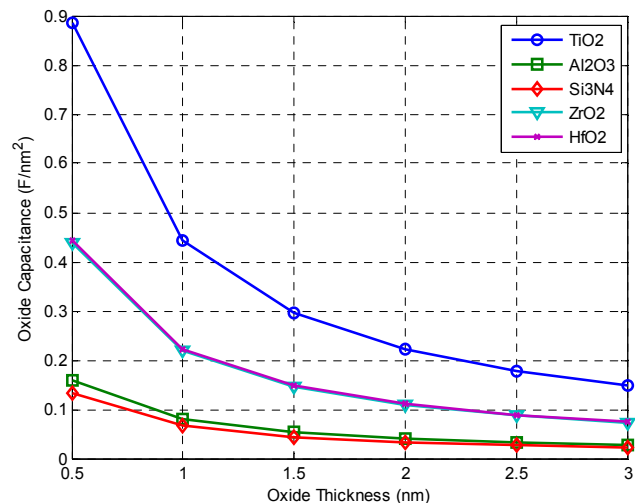


Figure 1. Oxide Capacitance of different insulating materials.

Table 1. Various Properties of Insulating Materials.

Properties of Insulating Materials	TiO <sub>2</sub>	Al <sub>2</sub> O <sub>3</sub>	Si <sub>3</sub> N <sub>4</sub>	ZrO <sub>2</sub>	HfO <sub>2</sub>
Thermal Conductivity (W/m-k)	7.4	40	29	2.2	1.1
Thermal Diffusivity (cm <sup>2</sup> /s)	0.0246	0.0817	0.1288	8.069 x 10 <sup>-3</sup>	9.47 x 10 <sup>-3</sup>
Dielectric Constant	50	9	7	24.7	25
Refraction Index	2.6142	1.7682	2.0458	2.1588	2.1114
Atomic Density (molecules/cm <sup>3</sup> )	3.2 x 10 <sup>22</sup>	1.8 x 10 <sup>22</sup>	1.4 x 10 <sup>22</sup>	2.8 x 10 <sup>22</sup>	2.8 x 10 <sup>22</sup>
Density (g/cm <sup>3</sup> )	4.23	3.95	3.17	5.68	9.68
Band Gap (eV)	9	8.8	5.3	5.8	5.8
CB Offset (eV)	3.2	2.8	2.4	1.5	1.4
Specific Heat (J/kg-k)	690	880	760	480	120
Melting Point (C)	1843	2072	1900	2715	2900
Coefficient of Thermal expansion (/K)	9.36 x 10 <sup>-6</sup>	5.2 x 10 <sup>-6</sup>	3.3 x 10 <sup>-6</sup>	10.5 x 10 <sup>-6</sup>	4.2 x 10 <sup>-6</sup>
Electron affinity(eV)	4.67	1.0	1.7	2.5	2

## 4. Effect of Insulating Materials on Leakage Current

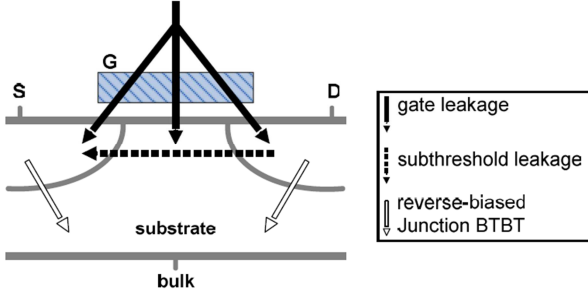


Figure 2. Major leakage mechanisms in MOS transistor.

Leakage current is dominated by subthreshold leakage, gate-oxide tunneling leakage and reverse-bias pn-junction leakage for nanoscale device like silicon technology based transistor and/or polycrystalline solar cell [21, 29]. Those three major leakage current mechanism are illustrated in Figure 2. There are still other leakage components, like gate induced drain leakage (GIDL) and punch through current, however, those ones can be still neglected in normal operation of digital circuits [19, 25-26].

### 4.1. Subthreshold Current

Supply voltage has been scaled down to keep dynamic power consumption under control. To maintain a high drive current capability, the threshold voltage ( $V_{th}$ ) has to be scaled too. However, the  $V_{th}$  scaling results in increasing subthreshold leakage currents. Subthreshold current occurs between drain and source when transistor is operating in weak inversion region, i.e., the gate voltage is lower than the  $V_{th}$ .

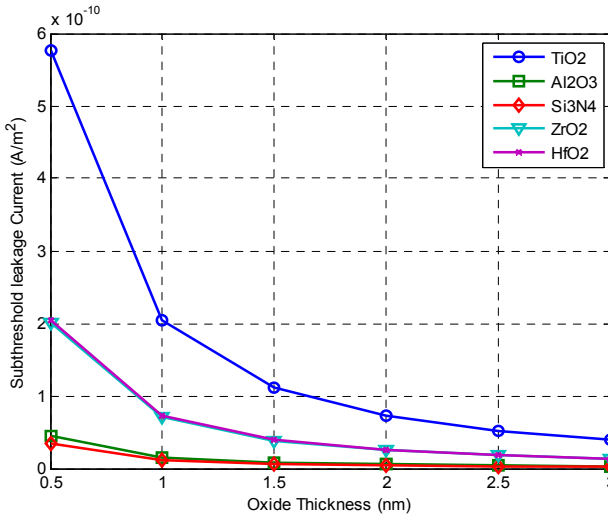


Figure 3. Subthreshold leakage current of insulating materials.

The drain-to-source current is composed by drift current and diffusion current. The drift current is the dominant mechanism in strong inversion regime, when the gate-to-source voltage exceeds the  $V_{th}$ . In weak inversion, the minority carrier concentration is almost zero, and the

channel has no horizontal electric field, but a small longitudinal electric field appears due the drain-to-source voltage. In this situation, the carries move by diffusion between the source and the drain of MOS transistor. Therefore, the subthreshold current is dominated by diffusion current and it depends exponentially on both gate-to-source and threshold voltage. The subthreshold leakage current [20] for a MOSFET device can be expressed as (1),

$$I_{\text{subthreshold}} = I_0 e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[ 1 - e^{-\frac{V_{ds}}{V_T}} \right] \quad (1)$$

where  $I_0 = W\mu_0 C_{ox} V_T^2 e^{1.8}/L$ ,  $V_T = kT/q$  is the thermal voltage,  $V_{th}$  is the threshold voltage,  $V_{ds}$  and  $V_{gs}$  are the drain-to-source voltage and gate-to-source respectively,  $W$  and  $L$  are the effective transistor width and length and  $n$  is the subthreshold swing coefficient.

### 4.2. Gate Oxide Tunneling Current

Aggressive scaling of the oxide thickness, in turn, gives rise to high electric field, resulting in a high direct-tunneling current through transistor gate insulator. The tunneling of electrons (or holes) from the bulk and source/drain overlap region through the gate oxide potential barrier into the gate (or vice-versa) is referred as gate oxide tunneling current. This phenomenon is related with the MOS capacitance concept. There are three major gate leakage mechanisms in a MOS structure. The first one is the electron conduction-band tunneling (ECB), where electrons tunneling from conduction band of the substrate to the conduction band of the gate (or vice versa). The second one is the electron valence-band tunneling (EVB). In this case, electrons tunneling from the valence band of the substrate to the conduct band of the gate. The last one is known as hole valence-band (HVB) tunneling, where holes tunneling from the valence band of the substrate to the valence band of the gate (or vice- versa). Each mechanism is dominant or important in different regions of operation for NMOS and PMOS transistors. For each mechanism, gate leakage current can be modeled by [21, 23].

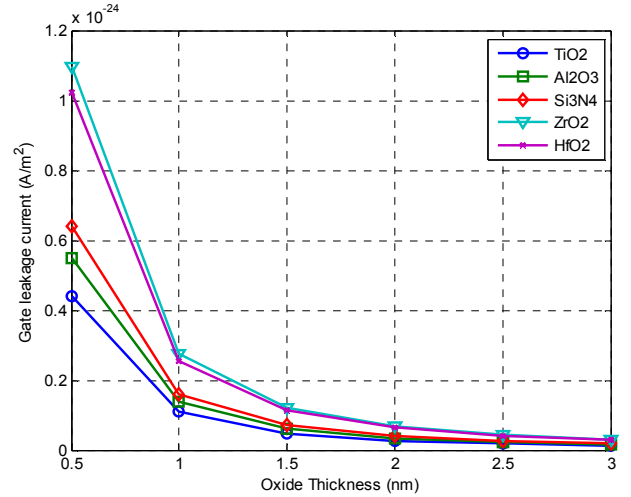


Figure 4. Gate leakage current of different insulating materials.

$$I_{\text{gate}} = WLA \left( \frac{V_{\text{ox}}}{t_{\text{ox}}} \right)^2 \exp \left( \frac{-B \left( 1 - \left( 1 - \frac{V_{\text{ox}}}{\phi_{\text{ox}}} \right)^{3/2} \right)}{\frac{V_{\text{ox}}}{t_{\text{ox}}}} \right) \quad (2)$$

where  $W$  and  $L$  are the effective transistor width and length, respectively.  $A = q^3 / 16\pi^2 \hbar \phi_{\text{ox}}$ ,  $B = 4\pi\sqrt{2m_{\text{ox}}}\phi_{\text{ox}}^{3/2} / 3\hbar q$ ,  $m_{\text{ox}}$  is the effective mass of the tunneling particle,  $\phi_{\text{ox}}$  is the tunneling barrier height,  $t_{\text{ox}}$  is the oxide thickness,  $\hbar$  is reduced Planck's constant and  $q$  is the electron charge.

#### 4.3. Band-to-Band Tunneling Current

The MOS transistor has two pn junctions – drain and source to well junctions. These junctions are typically reverse biased, causing a pn junction leakage current. This current is a function of junction area and doping concentration. When 'n' and 'p' regions are heavily doped, band-to-band tunneling (BTBT) leakage dominates the reverse biased pn junction leakage mechanism. A high electric field across a reverse biased pn junction causes a current flow through the junction due to tunneling of electrons from the valence band of the p-region to the conduction band of the n-region. Tunneling current occurs when the total voltage drop across the junction, applied reverse bias ( $V_{\text{app}}$ ) plus built-in voltage ( $\psi_{\text{bi}}$ ), is larger than the band-gap. The tunneling current density through a silicon pn junction is given by [21],

$$I_{\text{btbt}} = WLC \frac{\varepsilon V_{\text{app}}}{E_g^{3/2}} \exp \left( \frac{-DE_g^{3/2}}{\varepsilon} \right) \quad (3)$$

where  $C = \sqrt{2m^*q^3} / 4\pi^3 \hbar^2$ , and  $D = 4\sqrt{2m^*} / 3\hbar q$ ,  $m^*$  is the effective mass of electron;  $E_g$  is the energy-band gap;  $V_{\text{app}}$  is the applied reverse bias;  $\varepsilon$  is the electric field at the junction;  $q$  is the electron charge; and  $\hbar$  is reduced Planck's constant.

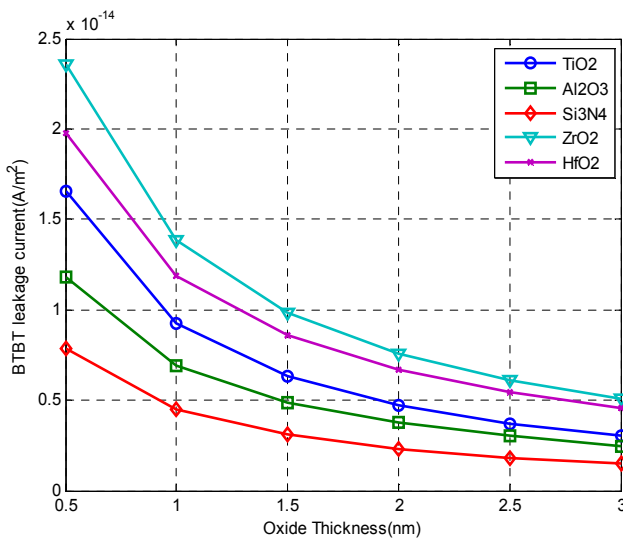


Figure 5. BTBT leakage current of different insulating materials.

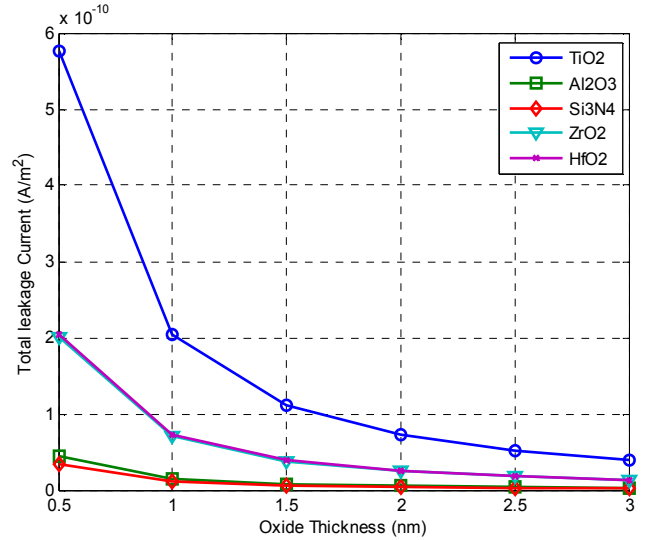


Figure 6. Total leakage current of different insulating materials.

Band-to-band tunneling leakage, negligible in current processes when compared to the subthreshold and gate oxide leakages, starts to be taken into account in 25nm technologies [22, 24].

## 5. Summary and Conclusion

Scaling of device dimensions has historically made advances in silicon ULSI technology. As a result of this scaling, both the vertical and horizontal dimensions have been reduced to a point where silicon dioxide as a dielectric material cannot satisfy the requirements. The many benefits driving manufacturers to use low-k dielectric materials include increased device speed, reduced power, required heat dissipation, and reduced interline talk. However, the transition to low k has been delayed primarily because of challenges in their integration, including etching and stripping problems associated with the carbon content materials.

Low-K materials in general exhibit weak polarization when subjected to an external electric field. There are several guidelines in formulating these materials; the most obvious one is the choice of a non-polar dielectric system. In these materials, polarity is weak because of symmetrical polar chemical groups that cancel the dipoles of chemical bonds between dissimilar atoms.

In the case of high-k materials, scaling the thickness of the gate dielectric has long been recognized as one of the keys to scaling devices. It is expected that for sub100 nm devices (CMOS) the gate oxide will be less than 2 nm. Thus it appears that SiO<sub>2</sub> will be unsuitable as a gate insulator in the sub-100 nm device. The vertical scaling requirements for gate stacks and for shallow extension junctions require 1 nm equivalent oxide thickness (EOT) to deal with leakage current tunneling. Some metal oxides, like HfO<sub>2</sub>, ZrO<sub>2</sub> and their silicates, have been identified as promising materials that are supposed to work with 1 nm EOT. However, integration of high-k



materials will be a challenging task because of the chemical bonding (ionic) and are likely to exhibit both ionic conduction and high charge levels.

The limited chemical and thermal stability are the two most important criteria associated with alternative high-k dielectrics and alternative gate electrode materials. In spite of the advantages of the polysilicon gate, the present process flow to integrate the future advanced gate stack employing these high-k materials is still questionable. Thus new integration schemes and device structures may be required to form source/drain junctions of MOS and all high temperature processes are to be done before the formation of the gate stack. At the same time, the chemical mechanical polishing (CMP) process used to planarize the surface has several advantages and challenges. The challenges include identifications of suitable materials for sacrificial gate stack and spacers and development of the consumables. Although several high-k materials and processes have been investigated, it still appears that the major concern is the cost.

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