
Hardware Implementation of Amplitude Shift Keying and Quadrature Amplitude Modulators Using FPGA

Tchahou Tchendjeu Achille Ecladore^{1,*}, Tchitnga Robert², Fotsin Hillarie Bertrand²

¹Department of Computer Engineering, University of Bamenda, Bambili, Cameroon

²Department of Physics, University of Dschang, Dschang, Cameroon

Email address:

tchahoutchendjeu@yahoo.fr (T. T. A. Ecladore), robert.tchitnga@univ-dschang.org (T. Robert), hbfotsin@yahoo.fr (F. H. Bertrand)

*Corresponding author

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Abstract: In our paper, we present the implementation of two kinds of FPGA-based modulators: ASK and QAM signal modulators. The ASK modulators we implemented are OOK, ASK, and 4ASK, then the QAM modulators implemented are 4QAM and 16QAM. The generation of the sine wave carrier is the main task when implementing any digital transmitter including ASK and QAM modulators. For us to implement these modulators, a sine function with floating-point operation as per IEEE754 standards is used based on Hardware Description Language technique. When the carrier is generated, the digital message modulates the amplitude of the carrier. To implement the QAM modulator, we need two sinusoidal carriers. A cosine function and a sine function are built to get the two carriers. Alongside to this work, ASK and QAM signal modulators are implemented using 26-bit phase accumulator and Look Up Table to generate the sine and cosine functions, then comparison of speed, occupied area and estimated power consume are done with the proposed modulators. Without using DSP builder tools or an Altera system generator, we implemented the whole systems using VHDL on cyclone IV-E-EP4CE115F29C7N of the board DE2-115. In general, the proposed modulator design present low area and power consumption than modulator using LUT or CORDIC.

Keywords: FPGA, ASK, QAM, LUT, Digital Modulator

1. Introduction

The development of programmable and reconfigurable devices has triggered the use of digital communication techniques in modern communication systems. One of the digital communication technique is the concept of radio-defined software (SDR). Joseph Mitola [1-3] was the first researcher who introduced the concept of radio-defined software by allowing the implementation of the radio (transceivers) programmable and reconfigurable. This technique is cost effective and presents some advantages like resistivity to the impairments, encryption, security, noise immunity, source coding, multiplexing of video, equalization, error detection and correction. The reconfigurable hardware platform is the main component on which any SDR is constructed. Most of the time, SDR are made up of FPGA,

RF mixers and filters, Digital-to-Analog Converter (DAC), and Analog-to-Digital Converter (ADC). The FPGA fund into SDR usually used to perform critical filtering and processing works on data rate interpolation or decimation. One of the challenges in digital communication techniques is to construct with FPGAs an entire SDR-based system. We are going to overcome this challenge, focus some of the research activity to carry out the implementation of digital modulators such as Frequency Shift Keying (FSK), Amplitude Shift Keying (ASK), Phase Shift Keying (PSK) and other digital modulators using Programmable Logic Devices. The work of Quadri and Tete [4] presents a summary of some research papers using Xilinx System Generator to implement digital modulator. The paper we just

cited is a good document to understand current achievements and future research directions. Some other examples are presented into this paper such work include; Erdogan et al presents the implementation of BASK (Binary ASK), BFSK (Binary FSK), and Binary (BPSK) modulators on FPGA development board using Verilog [5], the implementation on a SPARTAN-3 FPGA of a Binary PSK (BPSK) modulator and demodulator presented by Bhore and Sarde [6], the implementation of BPSK on Xilinx System Generator with the help of MATLAB SIMUINK presented by Popescu et al [7], and the design and implementation of a BPSK transmitter using Virtex-4 development board with the Digital to Analog Converter available on the P240 analogue module presented by Chye et al [8].

An FPGA-based implementation of different digital communication schemes using a SPARTAN-3 FPGA is presented Rajaram and Gayathre [9]; in this paper they use a CORDIC (Coordinate Rotation Digital Computer) algorithm to generate the sine wave carrier using the VHDL language. Rajaram and Gayathre did not use Xilinx System Generator or MATLAB SIMUINK as it is done in most of recent papers. A novel "all-digital transmitter" was extended by Zhuan Ye et al [10] to the software defined functionalities to radio frequency concept.

The all-digital transmitter is implemented using pulse width modulation (PWM) technics such that the digitalized RF (Radio Frequency) signal can be directly synthesized in the digital domain. The implementation PWM (pulse width modulator) using FPGA is made possible due to the low rate of the signal processing of PWM. When we combine a QAM modulator and an RF PWM, this demonstrates a real time QAM modular with numerical RF output signal using a realistic signalling format.

Varieties of FPGA development boards have been used to implement Analog modulators [11-17] as presented in the last few paragraphs for digital modulators. Optimized solutions for power consumption, efficiency and resources utilization are presented by some authors. More works are still needed despite all the progress.

The implementation of more complex modulation schemes through efficient design techniques and development of

optimum solutions is our focus in this work. We are presenting, in this manuscript a novel method of implementing an FPGA-based OOK, BASK, 4ASK, 4QAM, and 16QAM modulators using sinusoidal function generator build with 32 bits floating point of the IEEE754 standards for calculation as well as some other VHDL based functions.

The rest of the paper presents in section II the techniques of digital modulations, in section III the amplitude shift keying and quadrature amplitude circuit design, in section IV the simulation results, in section V the experimental results and the final section VI is the conclusion.

2. Techniques of Digital Modulations

The process that translates a baseband signal into the bandwidth of the medium is called modulation. In radio communications, adjusting a physical characteristic of a sinusoidal carrier is call modulation. The physical characteristics may either be the amplitude, phase, frequency or a combination thereof. At the transmitting end, a modulator is the device carrying out the process of modifying one of the carrier parameters and at the receiving end, a demodulator is there to reconstituted the original information. The block diagram show in the figure 1 is a digital transmission and reception chain. The digital input is the information to be transferred by a transmitter; it is encoded using particular parameters then sent into channel transmission. The modulator adjusts a physical characteristic of the local digital sinusoidal signal of higher frequency with the encoded low frequency signal to have a higher frequency range signal for an efficient transmission. The transmitted signal travels through the channel to reach the receiver end. The reverse operation is done at the receiver end. Once the modulated signal arrive receiver end, it is combined with the local digital sinusoidal signal to be demodulated by the demodulator block. The Decoder retrieve back, from the demodulated signal, the data in its original form. This process reproduces the transmitted information that was sent from the transmitter.

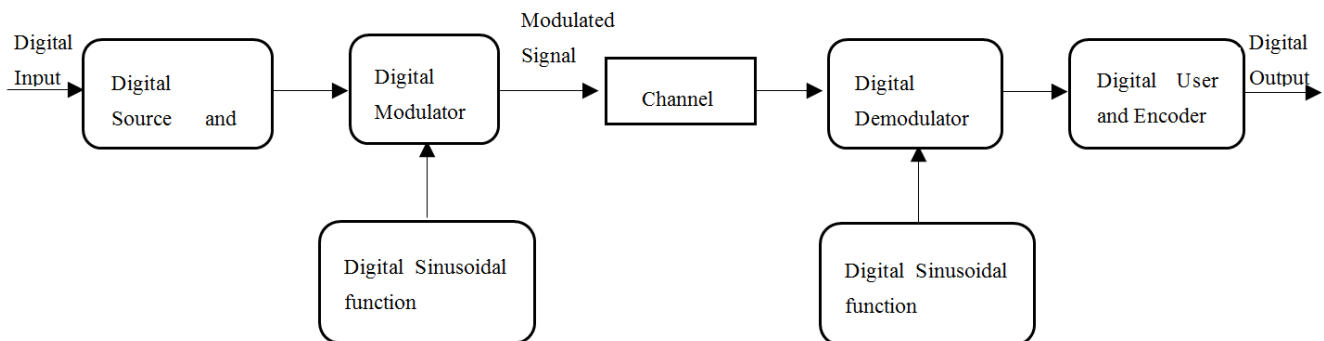


Figure 1. Digital Modulation Diagram.

3. Amplitude Shift Keying and Quadrature Amplitude Circuit Design

3.1. Sinusoidal Function Algorithm

Let consider $\theta_{deg} = 1^\circ$ and $\theta_{rd} = \pi/180 rd$, the discrete angles can be written as $m\theta_{deg}$ in degree and $m\theta_{rd}$ where $m = 0, 1, 2, \dots, 360$ for a complete circle. The sine function of these angles is $Sin[m\theta_{deg}] = Sin[m\theta_{rd}]$. A circle can be divided into four quadrants, so we can say that $Sin[m\theta_{deg}] = Sin[(k-1)\pi/2 + n\theta_{rd}]$. Where $k = 1, 2, 3, 4$ for the four quadrants and $n = \{0, 1, 2, \dots, 90\}$ the steps into a quadrant. From this, the discretization of the sine function can be done as follow:

a. For the first quadrant, $k = 1$ and $0 \leq m < 90$

$$Sin[m\theta_{deg}] = Sin[n\theta_{rd}] \text{ with } n = 0, 1, 2, \dots, 90.$$

b. For the first quadrant, $k = 2$ and $90 \leq m < 180$

$$Sin[m\theta_{deg}] = Sin[\pi/2 + n\theta_{rd}] = Cos[n\theta_{rd}],$$

this can be written as $Sin[m\theta_{deg}] = Sin[n\theta_{rd}]$ with $n = 90, 89, 88, \dots, 0$.

c. For the first quadrant, $k = 3$ and $180 \leq m < 270$

$$Sin[m\theta_{deg}] = Sin[\pi + n\theta_{rd}] = -Sin[n\theta_{rd}] \quad , \quad \text{with } n = 0, 1, 2, \dots, 90.$$

d. For the first quadrant, $k = 4$ and $270 \leq m < 360$

$$Sin[m\theta_{deg}] = Sin[3\pi/2 + n\theta_{rd}] = -Cos[n\theta_{rd}],$$

this can be written as $Sin[m\theta_{deg}] = -Sin[n\theta_{rd}]$ with $n = 90, 89, 88, \dots, 0$.

From the discretization, we can notice that $Sin[n\theta_{rd}]$ is the only value to be calculated for the whole circle. With this, the angle change is $0 \ll n\theta_{rd} \leq 1.57$. By using the Taylor series expansion with the first six polynomials to implement the sine function, we have the following:

$$\begin{aligned} Sin[n\theta_{rd}] &= n\theta_{rd} - (n\theta_{rd})^3/3! + (n\theta_{rd})^5/5! \\ &\quad - (n\theta_{rd})^7/7! + (n\theta_{rd})^9/9! \\ &\quad - (n\theta_{rd})^{11}/11! + (n\theta_{rd})^{13}/13! \end{aligned}$$

The use of Taylor series to calculate the sine function introduces error in the calculation. We have used MatLab to determine error between the build in sine function and the Taylor series expansion we are using. The error into the sine function using the proposed algorithm is shown figure 3.

From the details of the proposed algorithm of the sine function, an ASM chart (Algorithmic State Machine chart) is developed and presented in Figure 2.

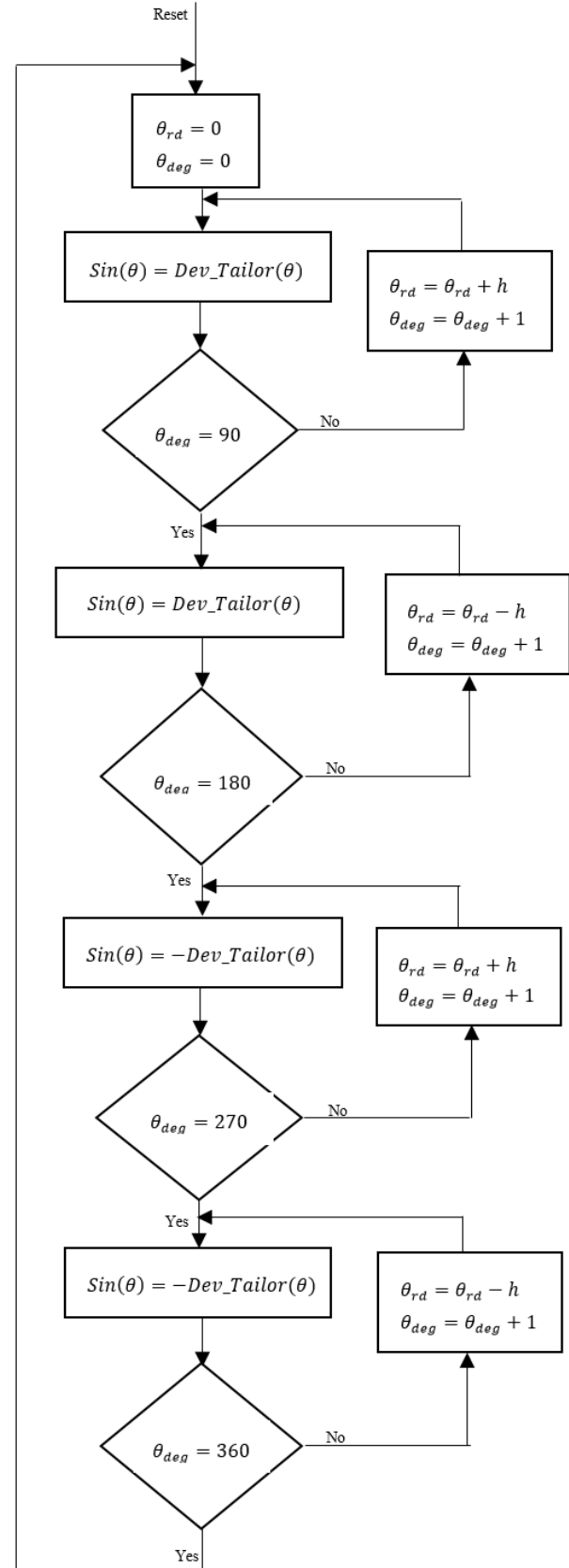


Figure 2. ASM chart of Sinusoidal function.

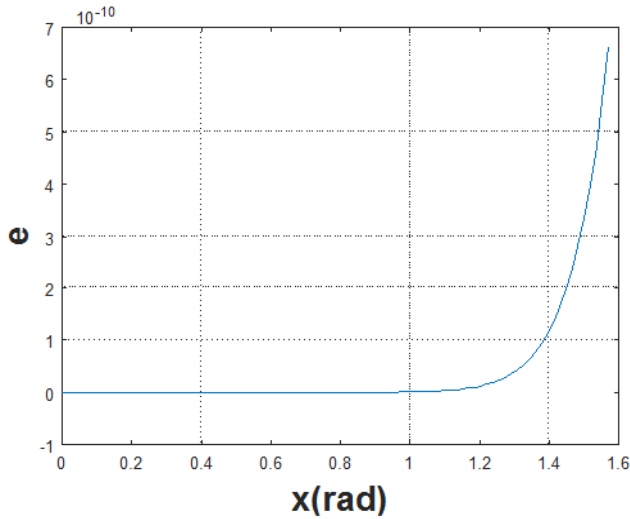


Figure 3. Error plot between the proposed sinusoidal function and the sinusoidal function of MatLab.

3.2. Amplitude Shift Keying Modulation Design

It is considered most of time that ASK is the simplest form of numerical modulation to be implemented. For the ASK modulator, the implementation consist of a digital sine wave generator, a multiplexer and multipliers as shown in Figure 3. During the implementation of the digital sine wave generator and the multiplexer, the floating point 32-bits in accordance with the IEEE754 standards is used to describe the behavior of this function in VHDL language. After the processing, the output signal is converted into standard bit vector. The output bit width can be chosen according to how smother we want the signal to be. The multiplexer selects to output a signal according to the message signal. If the message signal is the logic level “1” then the output signal is a sinusoidal signal. If the message signal is the logic level “0” then the output signal is 0 volt. This kind of ASK modulation is also known

as OOK (the coefficient $k=0$). The output of the ASK modulator was selected to be 16-bit for smoother signal during analog conversions and filtering. The 3T-model circuit [18] have been used to generate the message signal in the implementation. The message signal is a random binary signal that can represent input message or any signal capable to be converted into a binary format for transmission, such video, audio or computer data...

Many people do not consider the circuit of ASK we have described above with the coefficient $k=0$ as an ASK modulation. This is well-known as OOK. In this well-known OOK the output modulated signal sine wave with non-zero amplitude when the message is one and zero when the message is zero. In ASK, the modulated output signal is a sine wave taking on different discrete amplitude that can be selected based on the message signal. To implement this form of binary ASK (BASK), the value of the coefficient k is chosen between zero and one. For the message bit “1” the modulated output signal is the generated sine wave itself while for the message bit “0” the modulated output signal is the generated sine wave multiply by the coefficient.

Here we have chosen the coefficient to take the value of $k=0.5$. Using this same method of BASK modulation, a higher order ASK (M-array ASK) has been implemented. We implemented a 4-ASK modulator as presented in Figure 4. With this modulator, the message data is converted from serial to parallel to enable the proper functioning of the multiplexer circuit. The 4ASK modulator uses two bits to represents its symbols and three multipliers with three different coefficients $k1$, $k2$ and $k3$. The multiplexer circuit, hence, will have four input signals as it is shown in of Figure 4. The four different amplitudes are obtained using the following coefficients values: $k1=0.75$, $k2=0.50$ and $k3=0.25$.

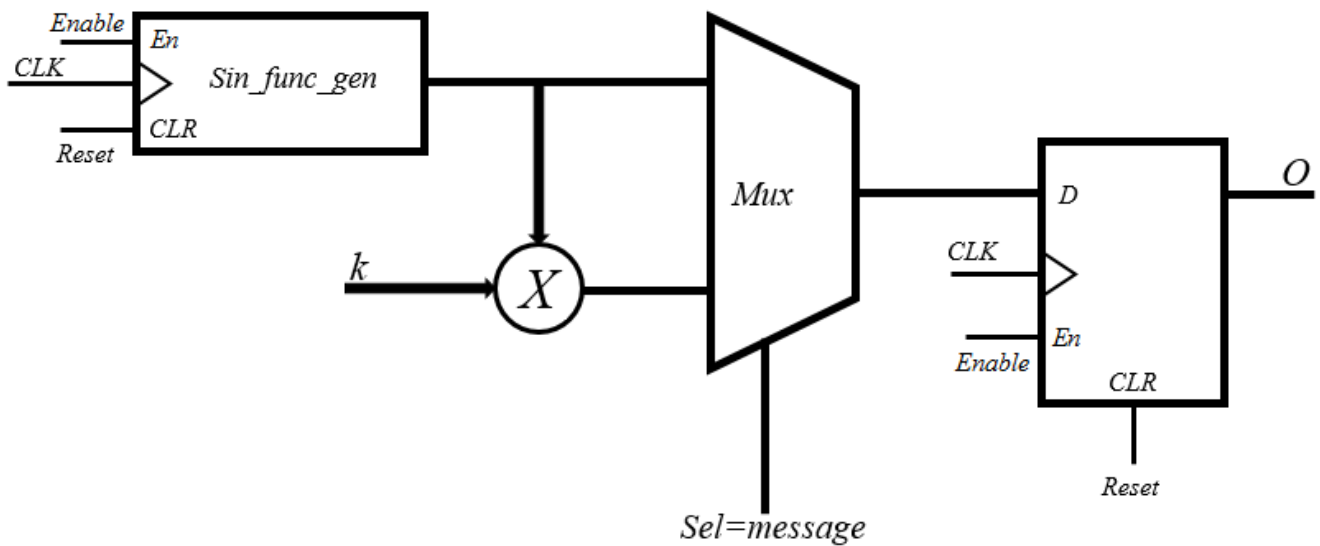


Figure 4. Proposed circuit design of ASK modulator.

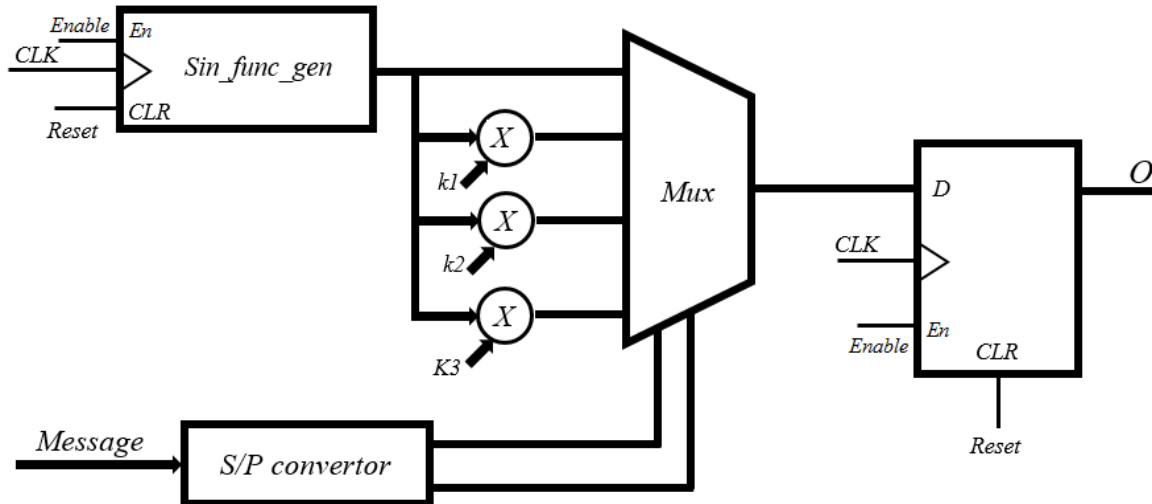


Figure 5. Proposed circuit design of 4-ASK modulator.

3.3. Quadrature Amplitude Modulation Circuit

In Quadrature Amplitude Modulation, based on the incoming bits stream, the amplitude of two carrier waves is being change. The cosine wave is the first carrier while the sine wave is the second. These two carriers are generated with the same frequency. In QAM, the output modulated signal has amplitude and phase variations. QAM is considered as a combination of ASK and PSK. The QAM modulator circuit we are proposing is shown at Figure 5. This proposed circuit is the simplest form of QAM modulation which is 4QAM. We also proposed the circuit of 16QAM shown in Figure 6. To implement this kind of modulator, we need two sinusoidal waves and they have a phase difference of 90-degree. Based on the algorithm describe in section 3.1,

we have proposed a cosine generator. These two generators produce sine and cosine functions to be used as carriers.

The circuit shown in Figure 5 and Figure 6 are directly described using VHDL language to be implemented. The development software used here is Quartus II 10.1 and the simulation done through ModelSim-Altera 6.5e. The 4QAM modulator looks similar to QPSK with some differences [19]. The main difference is that, we need two carriers only in 4QAM while in QPSK four carriers are needed. The multiplexer circuit of the QAM modulator receives four different carrier signals based on the combination of S_0 and S_1 . This multiplexer circuit selects one out of four different combinations of the two input carriers based on the incoming symbols of data as shown in Table 1.

Table 1. Representation of 4QAM symbol.

Constellation symbol	Modulated Signal	Constellation symbol	Modulated Signal
00	$S_0 + S_1$	10	$-S_0 + S_1$
01	$S_0 - S_1$	11	$-S_0 - S_1$

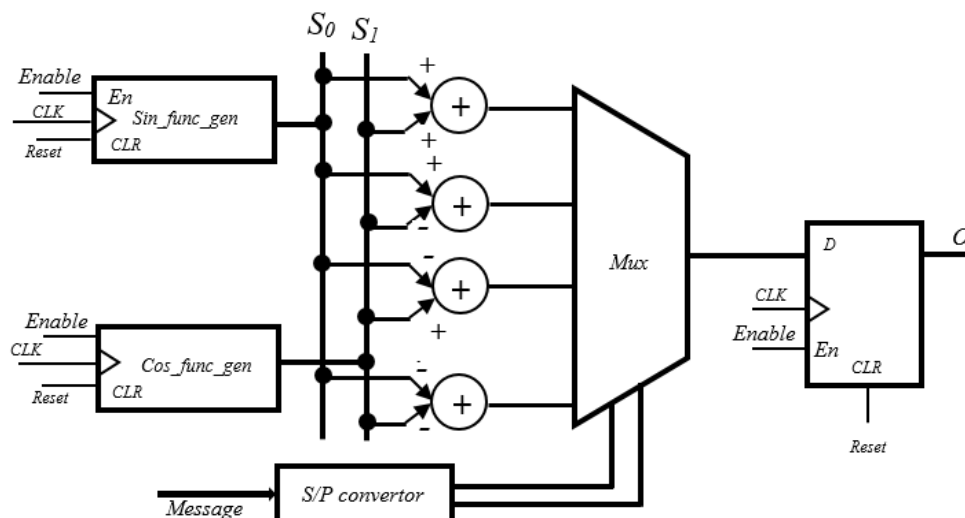


Figure 6. Proposed circuit design of QAM modulator.

From the implementation QAM we are now moving to the implementation of 16QAM modulator. Two carrier waves are used here and one multiplexer is needed for the implementation as illustrated in the circuit shown in Figure 6. The multiplexer and serial to parallel convertor blocks make the main differences between 16QAM and 4QAM

implementation. The circuit of serial to parallel convertor converts the incoming data into four parallel outputs for the 16QAM. The multiplexer circuit selects, based on the incoming symbols of data, one out of sixteen different combinations of the two input carriers as presented in Table 2.

Table 2. Representation of 16QAM symbol.

Constellation symbol	Modulated Signal	Constellation symbol	Modulated Signal
0000	S_0+S_1	1000	S_0-S_1
0001	$3S_0+S_1$	1001	$3S_0-S_1$
0010	$-S_0+S_1$	1010	$-S_0-S_1$
0011	$-3S_0+S_1$	1011	$-3S_0-S_1$
0100	S_0+3S_1	1100	S_0-3S_1
0101	$3S_0+3S_1$	1101	$3S_0-3S_1$
0110	$-S_0+3S_1$	1110	$-S_0-3S_1$
0111	$-3S_0+3S_1$	1111	$-3S_0-3S_1$

4. Simulation Results

In order to check whether the design works properly, we simulated the proposed circuits in Figure 3 to 6. We have used Quatus II 10.1 and ModelSim-Altera 6.5e to perform

the timing simulations. The results presented here, are some important information of the synthesis. A comparison is also done to compare the resource utilization of our proposed circuits and the circuit proposed by Amean & al [20].

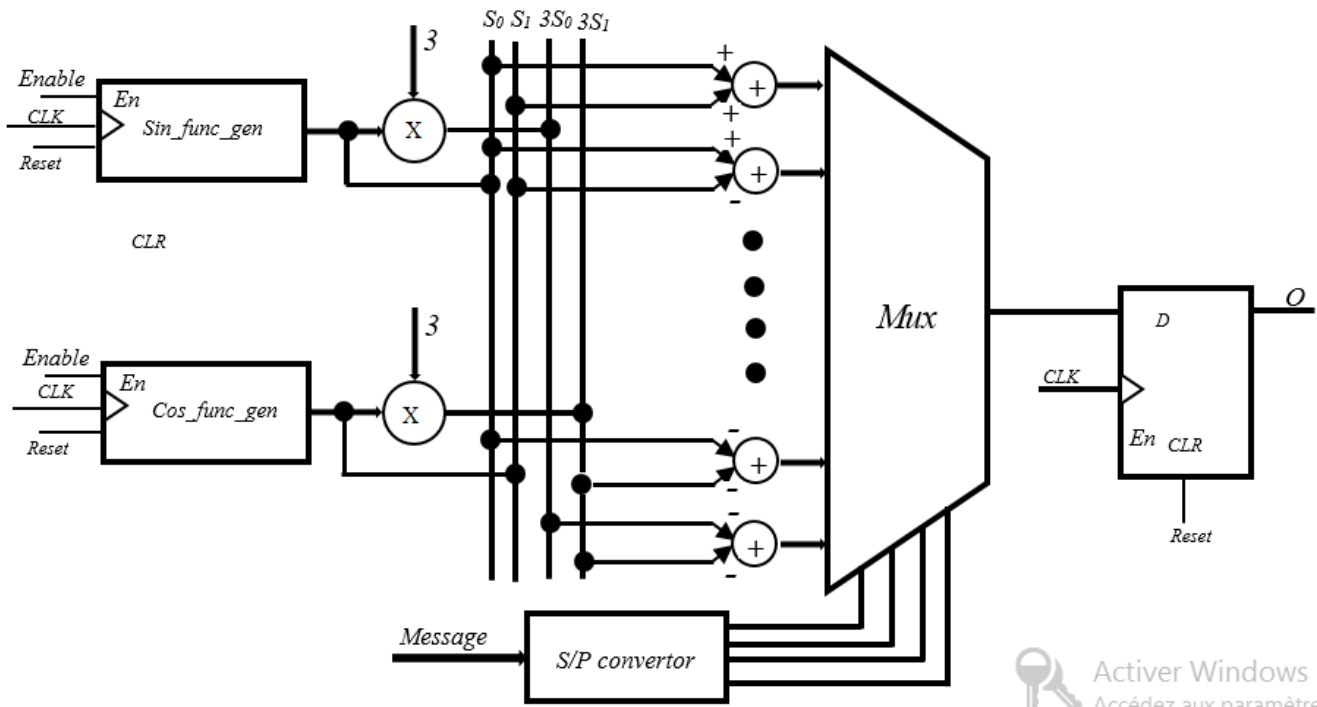


Figure 7. Proposed circuit design of 16QAM modulator.

4.1. RTL Schematics

The register transfer level (RTL) schematic of proposed ASK and QAM modulators are shown in Figure 7 and Figure 8 respectively. These two RTL design are achieved by describing into VHDL language each block. To generate the message for simulation of the modulators, the chaotic of

circuit of Tchitnga & al [21] was describe into VHDL to generate random numbers and then MatLab is used to convert these numbers into binary signal and save into a file text readable by VHDL. The “readfile” block we observe in RTL schematics are reading the message from the saved file and sending to the modulators.

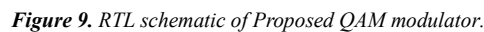
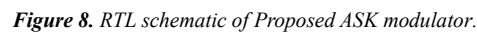


Figure 7 and 8 present the results of behavior simulation of the proposed ASK modulator using $k = 0$ and $k = 0.5$ respectively. Figure 9 present the results of behavior simulation of the 4ASK modulator. It can be seen that the level of the amplitude of the modulated signal depend on the nature of the bit to send.

The timing diagram shows a sequence of messages and a corresponding signal waveform. The messages are /ook_tchahou_top... and the signal is a square wave. The time scale ranges from 0 to 24,000 us.

Figure 11. Simulation behavior result of the proposed ASK modulator (BASK, $k=0.5$).

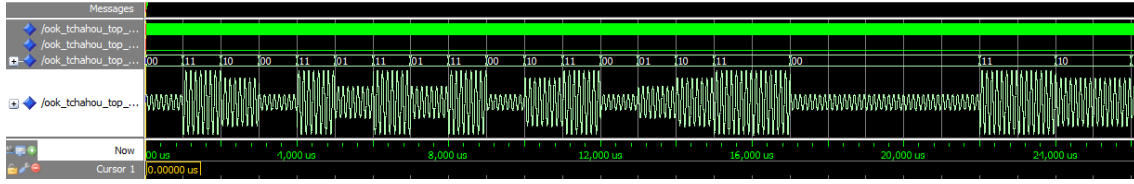


Figure 12. Simulation behavior result of the proposed 4-ASK modulator.

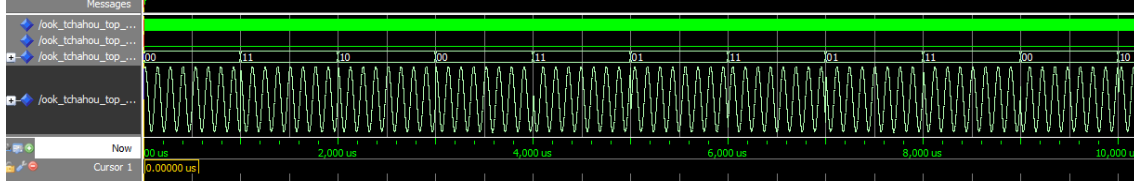


Figure 13. Simulation behavior result of the proposed QAM modulator.

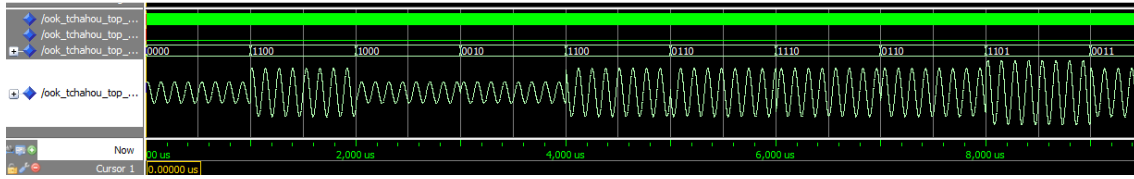


Figure 14. Simulation behavior result of the proposed 16QAM modulator.

4.3. Comparisons

An Altera chip is chosen for resources, power consumption and speed comparison between the proposed modulators and the circuit proposed in study of Al-Safi and Bazuin [20] using LUT to implement the sinusoidal functions. Table 1 denotes comparison of resources, power utilization and speed of ASK modulators using cyclone IV E EP4CE115F29C7N. Calculation of resources, power utilization and speed based on synthesis report shows that, the required resources (both logic elements and logic registers) of our proposed ASK modulators is greater than that of the design proposed in study of Al-Safi and Bazuin [20], the required resources (both memory bits and embedded multiplier) of our proposed ASK modulators is nil while the design proposed in study of

Al-Safi and Bazuin [20] is important, our proposed ASK modulators consume less power and are limited in frequency than design proposed in study of Al-Safi and Bazuin [20] (see Table 1). Table 2 itemizes resources, power utilization and speed of QAM modulators using cyclone IV E EP4CE115F29C7N. Our proposed QAM modulators consume less resources and power than that of the design proposed in study of Al-Safi and Bazuin [20]. We can notice here that, the design proposed in study of Al-Safi and Bazuin [20] are limited in frequency than our proposed modulators. Based on the design facility, resources and power consumption, our proposed modulators can be used to implement software-define radio.

Table 3. Resources, power consumption and Maximum Frequency comparison among LUT and Sin Function of ASK Modulators on Altera chips EP4CE115F29C.

	OOK Modulator		BASK Modulator		4ASK Modulator	
Resources	Ref20	Our Model	Ref20	Our Model	Ref20	Our Model
Logic elements	22	42	22	42	23	82
Total registers	22	30	22	30	22	58
Memory bits	4 096	0	4 096	0	4 096	0
Embedded multiplier	0	0	2	0	2	0
Frequency Max (MHz)	308.45	317.97	332.78	317.97	333	230.15
Power (mW)	138.78	138.05	138.78	138.05	140.05	136.35

5. Experimental Results

The experiment results were obtain in a laboratory with the use of the Altera development board DE2 115 and a VGA screen to visualize the wave form as presenred in Figure 15. The 3T-model circuit [18] to generate the message, the digital oscilloscope with VGA output and the modulator, all-digital design was implemented on the Altera DE2 115 board.

During design we fixed the data rate of the message at 1 Kb/s and the frequency of the sinusoidal waves at 7 KHz. For the implementation frequencies have been maintain. The implementation of all the proposed modulators (BASK, 4AKK, 4QAM and 16QAM) were realized using digital circuitry, as describe in section 3. The output of the modulators were connected directly to the digital oscilloscope added to the design for visualization through the VGA port of the Altera DE2 115 board. At the end, we

connected a monitor to the VGA port of the FPGA board in order to observe on real-time the analog OOK, BASK, 4ASK, 4QAM and 16QAM signals on a screen as presented

Table 4. Resources, power consumption and Maximum Frequency comparison among LUT and Sin Function of QAM Modulators on Altera chips EP4CE115F29C.

Resources	QAM Modulator		16QAM Modulator	
	Ref20	Our Model	Ref20	Our Model
Logic elements	220	78	220	78
Total registers	22	56	38	56
Memory bits	8192	0	8192	0
Embedded multiplier	0	0	0	0
Frequency Max (MHz)	86.72	241.7	80.72	2234
Power (mW)	149.53	135.58	148.64	134.4



Figure 15. Experimental set-up of the FPGA-based implementation of ASK and QAM modulator using a DE2 115 board and the VGA Screen.



Figure 16. Experimental result of the proposed 4-ASK modulator.



Figure 17. Experimental result of the proposed QAM modulator.

6. Conclusion

An FPGA implementation of OOK, BASK, 4ASK, 4QAM and 16QAM digital modulators were successfully performed on the targeted device cyclone IV E EP4CE115F29C7N of the FPGA board DE2 115. The main achievement of this piece of work is the implementation of a sinusoidal function generator into VHDL to generate the carrier instead of using LUT or CORDIC. The introduction of this sinusoidal function generator into these types of digital modulators has enable us to optimize the frequency limitation, the resources and power utilization. The proposed modulators are flexible and suitable for PFGA implementation of baseband-modulation as part of optical fiber transmission and software-defined radio system. This implementation can also be used for educational purposes in laboratories of

in Figure 16 and Figure 17. We can see that the real-time results and the simulation results are in good agreement.

digital communication to teach digital design and digital communications.

Declaration of Competing Interest

The authors declare that there is no known financial conflict or personal relationships that could have appeared to influence the work reported in this paper.

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