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Corner effect in multiplier SOI-FinFETs

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Abstract: SOI-Multi-FinFET was analyzed by a three-dimensional numerical device simulator and its electrical characteristics and potential distribution in the oxide and the silicon in the section perpendicular to the flow of the current were compared for single-fin, three-fin and five-fin FET to investigate the influence of fins number on corner effect in Dual-gate SOI Multi-FinFET, and we provide a comparison with a Tri-gate SOI Multi-FinFET structure.

Keywords: SOI, Fin FET, Corner Effect, Dual-Gate, Tri-Gate, Multi-Fin FET

1. Introduction

Recently, the Dual-gate structure has attracted a great deal of attention for its potential as a technology driver for sub-hundred-nanometer MOSFET. The two gates of a SOI-FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. Further, SOI-FinFET devices are built utilizing multiple parallel fins between the source and drain which introduces a large total channel width to achieve high transconductance, maintain good noise and mismatch performance [1]. Fig.1 (a) shows a structure of a multi-FinFET. This device consists of a thin silicon body, the thickness of which is denoted by T-Si, wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a FinFET is 2 *nh*, where *n* is the number of fins and *h* is the fin height.

Thus, wider transistors with higher on-currents are obtained by using multiple fins. The *fin* pitch (p) is the minimum pitch between adjacent *fin* s allowed by lithography at a particular technology node. Using spacer lithography, *p* can be made as small as half of the lithograph y pitch [2].

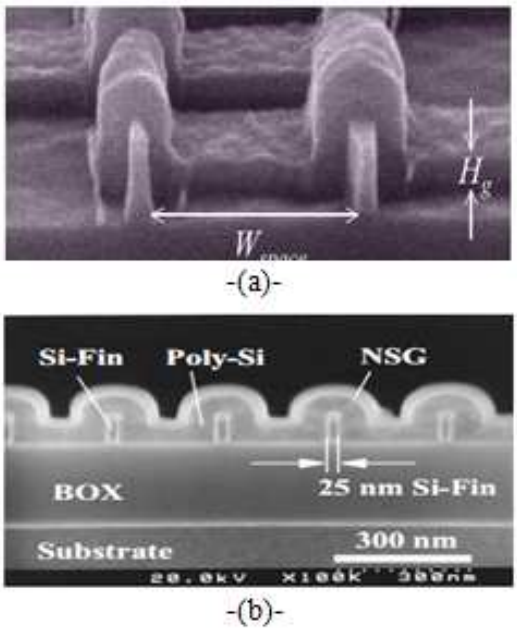

Figure 1: *(a) Multi-Fin Device, (b) Cross-sectional SEM image of the fabricated Multifin-FET with 5-Fins [3]*

Fig.1(b) shows the cross-sectional SEM image of the fabricated SOI-five-fin-FET. It should be noted that the widths at the top and bottom of the Si-Fin is entirely the same i.e., the Si-Fin shows the ideal rectangular channel shape.

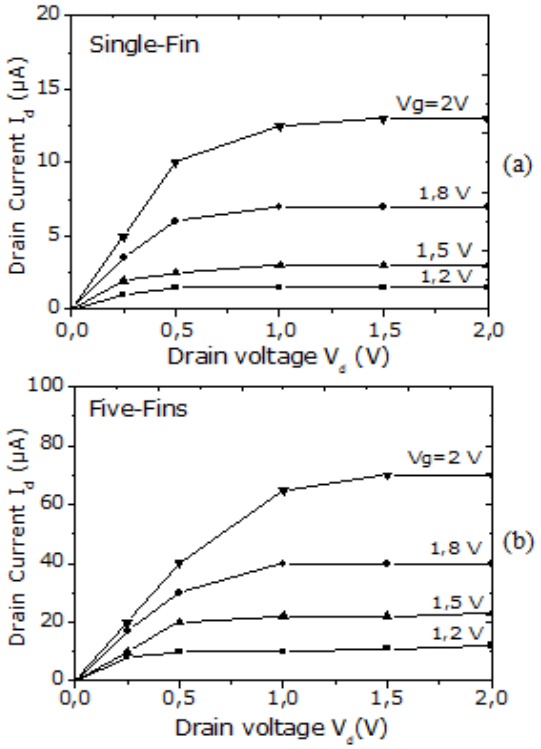

Fig.2. *I_d-V_d Characteristics of the fabricated SOI-Multifin FET a) - Single Fin; b) - Five-fin*

Fig.2 show the measured I_d-V_d characteristics for a three-gate SOI-Multi-FinFET structure with a single-Fin (a) and five-Fins (b) by TCAD Silvaco simulator for a 20 nm thick, 40 nm high Silicon fin, 25 nm for channel length and 2 nm for the gate oxide thickness with several gate voltages 1.2, 1.5, 1.8, and 2V.

It is apparent that 5 times of the drain current is accurately obtained in the five-Fin device compared with that of in the single-Fin device at a fixed gate voltage and drain voltage.

2. Corner Effects

Figure.3 show the corners witch present leads to the formation of independent channels with different threshold voltages. This phenomenon is known as corner effect and it needs to be suppressed by additional corner implantation and/or corner rounding [4-5]. Corner implantation uses the fin formation hard mask and allows a retarget of Tri-Gate threshold voltage independent of the halo implantation shared with the planar MOSFETs. The radius of curvature of the device electrical characteristics and can decide whether or not a different threshold voltage will be measured at the corners and at the planar interfaces of the device [6]. However, corner rounding erases electric field overlapping of Top- and Side-Gate and permits a homogenous transition between Top-and Side-Channel [5].

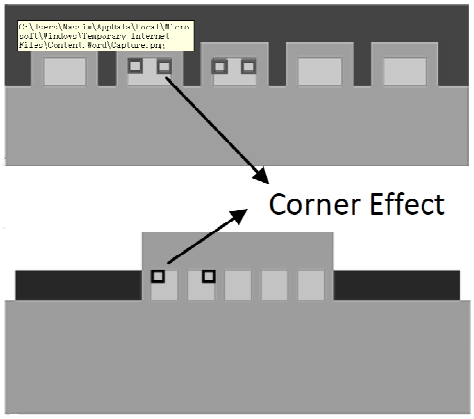

Figure 3: *Cross section view of the Five fin SOI-FinFETs showing the channel regions and corners: Double-gate (a); Triple-gate (b).*

3. Simulation and Results

We first optimize a single-finFET which then will be used as a base transistor for a multi-fin structure [7].

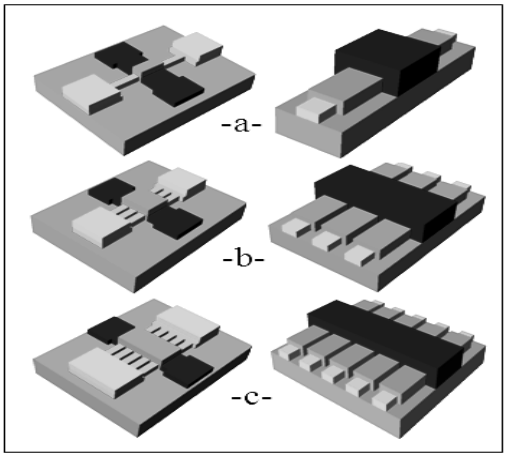

Figure.4: *3D Structure of SOI-Multi-FinFET a) Single-fin; b)Triple-fins; c) Five-fins.*

The bulk is lightly doped 10^{18} cm^{-3} to avoid the dopant fluctuation.

With extensive calibrated TCAD Silvaco simulations [8], we present results for a comparison of the potential in the oxide and the silicon in the section perpendicular to the flow of the current for various numbers of *fins* from n=1fin to 3 fins and finally 5 fins in the case of dual-gate SOI-Multifin FET and we will compare these results with the case of tri-gate SOI-Multifin FET as shown in (fig.4.a.b.c). In the case of SOI-Single-FinFET, the potential distribution shows that the potential barrier between the source and the drain is higher, and that the barrier is the highest in the middle of the channel which should push the electron flow from source to drain to the corners of the fin. Further, electric field from the substrate electrode penetrates into the channel decreasing the potential in the fin. This increases the source to-drain potential barrier in every part of the channel.

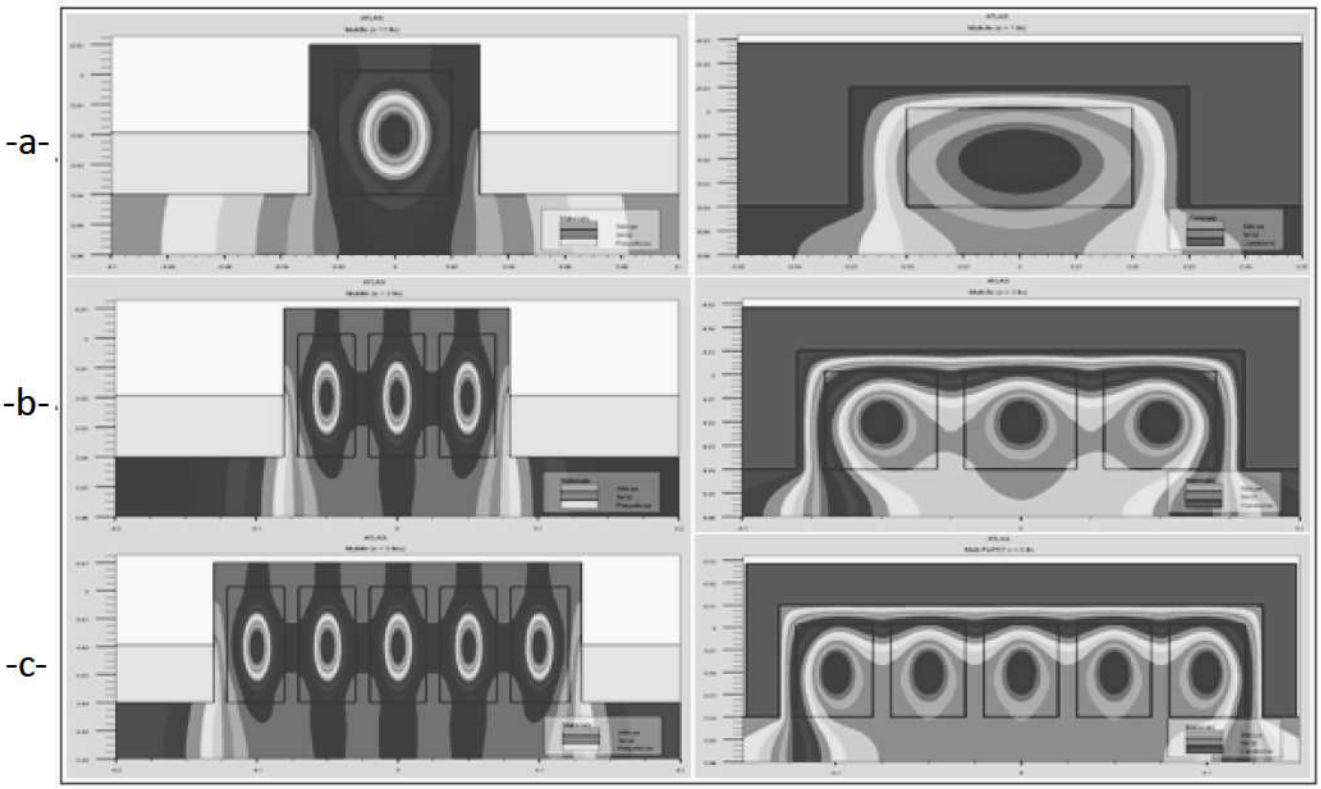

Figure 5: *Potential in the oxide and the silicon in the y-z section for the Dual-gate and tri-gate Multifin-FET (Vgs=0.5V) -a-Single fin -b- Three fins -c-Five fins*

It can be seen that the barrier rises from top to the bottom of the channel and it is the highest in lower part of the channel, around the bottom of the gate.

Higher barrier at the bottom and in the middle will force the electron flow to the top of the fin, or to be more precise, to the upper corners of the fin. For both Dual and Tri-gate SOI-Single FinFET, it can be seen that the current flow is pushed to four corners (4-corner effect), this means that if we will increase the number of fins, we will multiply these four corners effects by this new number, which will result an on-state drain current *n* times higher than single fin where *n* is the new fin number. Although Dual and Tri-Gate SOI-Multi-FinFETs have a completely identical doping in the active area, the performance of the tri-gate transistor is better than the one of the double gate transistor, because the Tri-gate has a slightly higher on-current, but simultaneously a much lower leakage current compared to the Dual-Gate, because the upper part of the fin also contributes to the total current of the open double gate transistor. A slight enhancement of the current in the corners of the fin in the open transistors is observed for both transistors considered.

4. Conclusion

Although SOI-FinFETs have aforementioned advantages, they also bring some other disadvantages, such as corner effect in relation to the multiple-gate structure. In contrast, the corner effect improves the performance of the FinFETs since the on-current is enhanced at the corners and the leakage current is suppressed. Since the corners effect is located at each fin, with increasing the fin number the influence of the corner effect became stronger and the leakage currents is more higher in shallow trench isolated CMOS transistors. Due to positive influence of the corner effect, the triple gate wrap around design of the SOI-Multi-FinFET appears to be more advantageous in comparison to the double gate design.

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