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Design of analog field programmable cmos current conveyor

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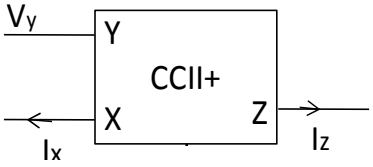
Abstract: The paper propose a modified high frequency current controlled current conveyor CMOS circuit CCCII where current gain, current controlling intrinsic impedance and circuit offsets are programmable independently to desired values within a specific field range after fabrication with the help of field programmable floating gate transistors FGMOS. The programmable charge at floating-gate of FGMOS using external voltages results in its threshold voltage variation, which in turn program the design (CCCII) specifications. The circuit occupies low power, about 1.509mW total power dissipation and shows higher temperature stability (0.0287uA/°C variation in output current with temperature change). With specific sizing and biasing condition, the current gain can be programmed from 0.2 to 2.1, intrinsic impedance from 15K to 51K, while offset current can be compensated, independently using each FGMOSFETs, respectively, with 13-bit precision. However the final programmable CCCII circuit with FGMOSFETs occupies 65µm × 54µm chip area. The circuit finds application in systems where field-programmability of the design using smaller sized hardware is required like universal filter, current control high frequency oscillator, etc as compared to the circuits using current control conveyor based FPAAs.

Keywords: Current Controlled Conveyor, Floating-Gates, Field Programmable Specifications, Field Programmable Threshold Voltage

1. Introduction

With CMOS scaling down, to maintain integration suitability current mode devices are finding more consideration in circuit designs. As supply voltage has become the great concern in present electronic design scenario especially for portable, battery powered equipment. Thus current-mode circuits like current conveyors are better suited for such purpose in comparison with voltage-mode ones. Current conveyor is a versatile analog circuit building block that offers an alternative method of implementing analog systems which traditionally have been based on voltage op-amps. It is a three terminal analog device which acts as an amplifier with unity gain without any overall negative feedback (between output Z and input X of figure 1 (a)), rather than the ill-defined open-loop gain and closed loop gain-bandwidth conflict of negative feedback voltage op-amp [1]. Thus the CC based amplifier does not depend critically on the matching of external components, instead depends only on the absolute value of a single component. It can provide a higher gain over a larger signal bandwidth under small or large signal conditioning than corresponding op-amp circuits [2]. Although the CC concept has been around for a long time with the first generation CC (CCI) proposed in 1968 and the more versatile and adaptable second generation CCII in 1970 [3, 4]. In CCI both the currents and the voltages in ports X and Y are forced to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z. Whereas in CCII input Y draws no current and Figure 1 (b) also depict its voltage-current describing matrix. With higher accuracy, bandwidth and because of the combined voltage and current properties in CCII circuit, it may be used to synthesize a number of analog circuit functions which are not so easily or accurately realizable using op-amp [5, 6]. However a major shortcoming of CCII is that it cannot control the parasitic resistance at X (R_x) thus, when it is used in some circuits, it must unavoidable require some external passive components, especially resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and no electronic controllability. Thus second generation current controlled current conveyor CCCII have

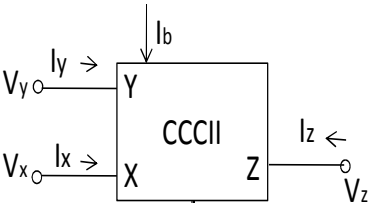
been introduced which provide electronic adjustability (illustrated via voltage-current matrix of CCCII circuit in Figure 1(c)) over CCII [7-11]. It allows implementation of electronic functions, usable at high frequency. Moreover, the current controllable resistance R_x is usable for the applications of tunable circuits. Therefore, this conveyor becomes useful in high frequency applications filtering [12] and, oscillator [13].



(a)

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 000 \\ 1\,00 \\ 0\ \pm 1\ 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

(b)



(c)

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0\,0\,0 \\ 1\ R_x\ 0 \\ 0 \pm 10 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

(d)

Figure 1. *(a) shows schematic of CCII. (b) CCII, I-V describing matrix. The voltage at the low impedance input X follows that at the high impedance input Y, while the input current node X is mirrored or 'conveyor' to the high-impedance output node Z. The +- sign indicates the polarity of the output current w.r.t the input current. (c) Schematic of CCCII (d) CCCII, I-V Matrix. The I_b is biasing current, by which the voltage relation between terminal X and terminal Y is adjusted. R_x shows parasitic resistor of terminal X and it is a function of I_b. The parasitic resistance Rx of terminal X is proportional to 1/ I_b.*

Now, as analog devices/circuits lack in accurate prototyping of the design, reconfiguring ability and automation, programmable devices like Field Programmable Analog Array (FPAA) have been developed. A FPAA is an integrated circuit, which can be configured to implement various analog functions using a set of configurable analog blocks (CAB) and a programmable interconnection network, and is programmed using on-chip memories [14]. The CAB can be implemented using different analog active circuits like a tunable unity gain frequency op-amp[14], programmable operational transconductance amplifier(OTA)[15], or programmable current conveyor [16]. The design challenges of the FPAA are mainly the CAB active circuit and the interconnection network. If the active circuit is programmable, then the FPAA user can implement tunable analog circuit applications such as on-chip tunable filters and variable gain amplifiers. Due to design complexity of op-amp based programmable active circuits they are not the efficient for most of the FPAA design. However tunable OTA using pre-defined set of control voltage signals, based FPAA design requires extra hardware to save the control voltage values [17]. In addition, digitally programmable fully differential second generation current conveyors (DPCCII) are also used in FPAA with an advantage of no additional circuitry for interconnections [18]. Various techniques are used to program CCII, first one was using a current division network (CDN) added in cascade with current follower [19]. The CDNs require current sources for biasing and maintaining circuit transistors in saturation region, thus increases circuit power consumption. Second approach was using current mirror to scale the current at Z port, however, this method can subject to transistors mismatching problems [20]. Third approach was using 3bit MOS R-2R ladder current division network, in which current scaling factor changes with 3-bit digital codeword applied to CDN [18]. Furthermore, various current mode reconfigurable analog modules were also proposed using low voltage digitally programmed current conveyor (DPCCII), where 4-bit control word is considered [20]. These digitally control designs had improved the on chip control of continuous time systems with reconfigurability but these designs experience limitation in applications where low power consumption, small size hardware, high resolution and continuous/analog programming instead of digital switching are required, like in highly integrated portable electronic devices. There are various electronic systems where high precision tuning ability/programmability is required like for biologically inspired circuits such as bionic ear processor, learning circuits and related adaptive filters, neuromorphic and cellular computing circuits, etc. However as illustrated earlier, CCCII has an advantage of tuning ability over CCII, whereas on-chip programming ability with the help of bias current will bring changes in the circuit operating conditions or rather result in circuit offsets. Programmable CCCII based FPAA can bring paradigm shift in programming and implementing electronics for above mentioned areas.

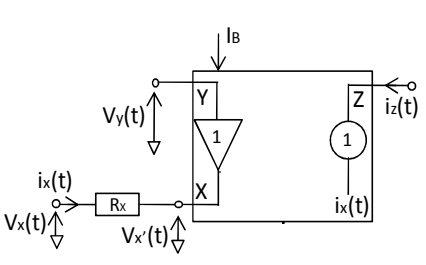
Thus to introduce continuous programming ability in CCCII design, we propose a comprehensive design procedure which allows post fabrication and independent tuning of critical specifications to desired values within a specific field range using analog voltages. In our proposed design flow instead of repeatedly iterative simulation steps to achieve very precise design specifications by fine tuning the W/L ratios of the FETs, we use first order classroom equations to achieve central value of desired specifications and then execute a customized fine tuning of specifications to the customers requirement. While maintaining small size and low power consumption FGMOS are introduced in place of conventional MOS device with which conductivity of a MOS can be corrected by altering its threshold voltage (V_T) by a field user [21, 22]. The CCCII circuit is analyzed

and derived in terms of design specifications whose derived equations show direct dependence on MOS thresholds. FGMOS offers continuous variation in threshold by storing the weights in a non-volatile analog memory with high accuracy [23, 24, and 25]. And the charge once stored at FG can be retained for more than 10 years. Thus a FPAA based on our proposed analog programmable CCCII design will not required extra hardware for storing, no digital code controlling circuitry however it will require interconnects to provide desired analog voltages to program floating gates of respective FGMOSs. In paper, parametric analysis of each design specification with respect to each FGMOS is performed and circuit is modified to achieve independent programming ability of design specification as well as circuit offsets, using respective FGMOSs. The total power dissipation and thermal stability of the modified design is also being catered in the paper. Such consistent approach to introduce programmability can be applied to various analog ICs (the idea of programmability using floating gate transistor is being published in conferences before [26, 27 and 28]).

2. Design Objectives

Before designing or introducing programmability in CCCII CMOS circuit, few design objectives need to be considered. Firstly the variation in the design specifications should be large and continuous. Indirect, non-volatile and high precision programming of FGMOS thresholds can produce large range and continuous programming of specifications. However, large continuous variation in specifications is difficult and sometimes unstable. Second design objective is that the variation of each specification should be independent of the other i.e., each specification should be programmed either by one or more FGMOS but should not alter any other design specifications. However if specification programming are not independent then either through modifying the circuit or by compensating the affected specification value using different set of FGMOS, should be prepared. Thirdly, operating point of the circuit should not alter too much during programming, i.e. current density in each transistor should not change significantly or in other words offset current should not vary significantly.

3. Basic CCCII Circuit Design



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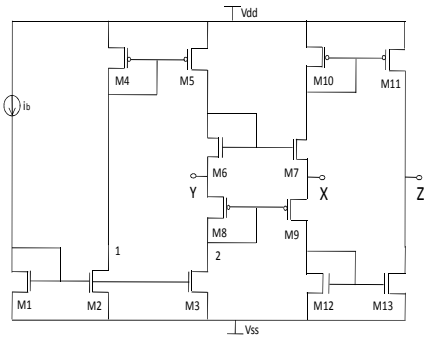

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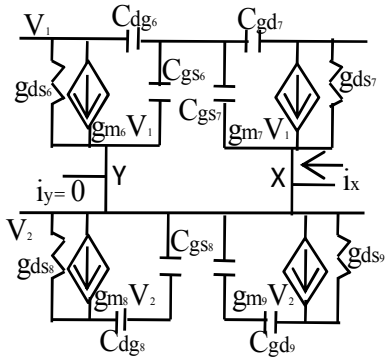


(c)

Figure 2. *(a): Equivalent circuit of an ideal CCCII [5] (b): Circuit diagram of CMOS CCCII [5] (c) High frequency small signal equivalent circuit of mixed Translinear loop of the CCCII circuit.*

The CMOS CCCII design [13] consists of four symmetric current mirrors and a mixed Translinear loop with one low impedance input (controlled by bias current), one high impedance input, one high impedance output, a suitable element for both voltage-mode and current-mode circuits. It basically consists of four current mirrors and a mixed Translinear loop. Equivalent circuit of an ideal CCCII is shown in Figure 2(a). It gives a high impedance input at port Y and a low impedance input at port X. With low magnitude input current i_x (t), the mixed Translinear loop force the drain current of its each transistor equal to I_b. Consequently, it gives $V_x(t)=V_y(t)$, (voltage follower represented in Figure 2(a)). Hence, the equivalent voltage follower presents at port X a small signal intrinsic resistor R_x that is inversely proportional to the square root of the bias current I_b (as derived from high frequency small signal equivalent model and expressed in equation (1) and (2) in next section). The two complementary current mirrors allow to duplicate on port Z the input current at X, thus $i_z(t)=i_x(t)$ (Current follower action between X and Z). Figure 2(b) shows the circuit diagram of CMOS CCCII referred from paper [5] and Figure 2(c) represents high frequency small signal equivalent circuit of mixed Translinear loop of the CCCII circuit.

3.1. High Frequency Small Signal Analysis

The CCCII design is operated at high frequency; accor-

dingly high frequency small signal equivalent model is generated and design characteristics are derived. The bias current I_b is mirrored equally to two nodes of the mixed Translinear loop, node 1 & node 2, as shown in Figure 2(b). NFET and PFET current mirrors are replaced by their respective small signal model in the Translinear loop as shown in Figure 2(c). The input current from port X is then mirrored using PFET and NFET current mirrors (M10, M11 and M12, M13), to the output port Z. From the small signal equivalent circuit of the design, current gain ($i_z(t)/i_x(t)$), voltage gain (V_x/V_y), intrinsic resistance R_x, output impedance R_{out} and dc offsets at X and Z has been derived and derived expression are as follows. Resistance R_x, using Thevenin theorem at port X, is given by:

$$R_X = \frac{1}{g_{m7}+g_{m9}} \tag{1}$$

where, transconductance gm7 & gm6, can be expressed in terms of square root of their respective saturation drain currents,

$$g_m = \frac{k_n' W/L}{2} \left(\sqrt{\frac{I_b}{k_n' 2W/L}}\right. \tag{2}$$

Thus, Rx is inversely proportional to the square root of the bias current Ib. The voltage gain (Vx/Vy) across port X and Y in the design is expressed as:

$$A_v = \frac{(s(C_{gs6}+C_{gs7})+g_{m6}+g_{m7})(sC_{gd2}-g_{m2})(sC_{gd5}+g_{m5})}{(g_{m7}+sC_{gs7})(sC_{gd2}+g_{ds2})(sC_{gd5}+g_{ds5})} \frac{V_b}{V_Y} - \frac{(g_{m6}+sC_{gs6})}{(sC_{gs7}+g_{m7})} \tag{3}$$

where, Vb is the voltage across the bias current Ib of the circuit. Moreover, current gain Ai =iz(t)/ix(t), assuming id6 = id7 = id8 and id9 = id7 + ix , is expressed as:

$$A_i = \frac{(sC_{gd5}+g_{m5})(sC_{gd2}-g_{m2})}{(s(C_{gd5}+C_{gs5}+C_{gs4})-g_{m4})(s(C_{gs1}+C_{gs2}+C_{gd2})+g_{m1})} \frac{I_b}{i_x}$$
$$\left[\frac{sC_{gd11}+g_{m11}}{(s(C_{gd11}+C_{gs10}+C_{g11})-g_{m10}} - \frac{sC_{gd13}-g_{m13}}{(s(C_{gs12}+C_{gs13}+C_{gd13})+g_{m12}}\right] - \frac{sC_{gd13}-g_{m13}}{s(C_{gd13}+C_{gs13}+C_{gs12})+g_{m12}} \tag{4}$$

Output impedance at port Z from small signal equivalent circuit of the CCCII design is being derived as:

$$R_{out} = \frac{1}{(g_{ds2}+g_{ds3}+g_{ds5}+g_{ds7}+g_{ds9}+g_{ds11}+g_{ds13})+ s(C_{gd2}+C_{gd3}+C_{gd5}C_{gd7}+C_{gd9}+C_{gd11}+C_{gd13})} \tag{5}$$

The graphs representing Rx variation with bias current Ib and frequency response of current gain and voltage gain are shown in Figure 3(d). Moreover, DC offset voltage at X and offset current at Z can be expressed by neglecting all parasitic capacitances in the expression (3) and (4) with no input voltage Vy or input current ix(t), respectively. Hence the output offset voltage at X is given by:

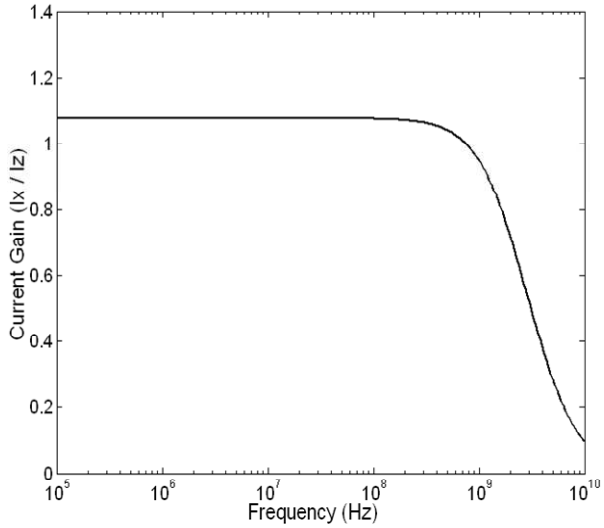
$$V_{offset} \cong -g_{m2}g_{m5}(g_{m6}+g_{m7})V_b \tag{6}$$

and output offset current at Z is given by:

$$I_{offset} \cong \frac{g_{m5}g_{m2}}{g_{m1}g_{m4}}\left[\frac{g_{m13}}{g_{m12}} - \frac{g_{m11}}{g_{m10}}\right] I_b \tag{7}$$

3.2. Characteristics of Basic CCCII Design

The proposed programmable modified CCCII design is simulated and its basic functionality with central value of specifications at specific biasing and sizing conditions of the circuit is estimated. The design characteristic plots like frequency response of current gain and voltage gain is represented in Figure 3(a) and (b). Figure 3(c) shows the input current i_x (800MHz frequency and 10uA amplitude sine wave) and the output current i_z. The graph in Figure 3(d) proves that the resistance R_x is inversely proportional to I_b. It shows theoretical and simulated values are in good agreement. The intrinsic resistance R_x varies from 21.194kΩ to 21.338kΩ when I_b is varied from 1.5mA to 0.5mA. Figure 3(e) demonstrates the variation in output current with change in temperature from -40°C to 80°C.



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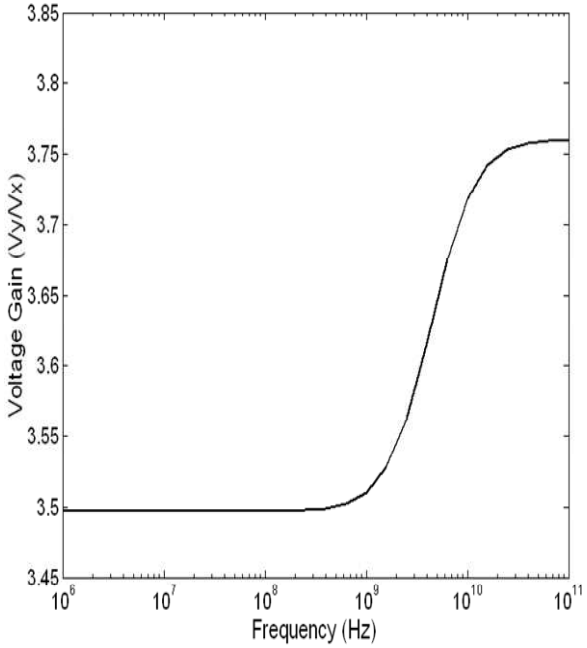

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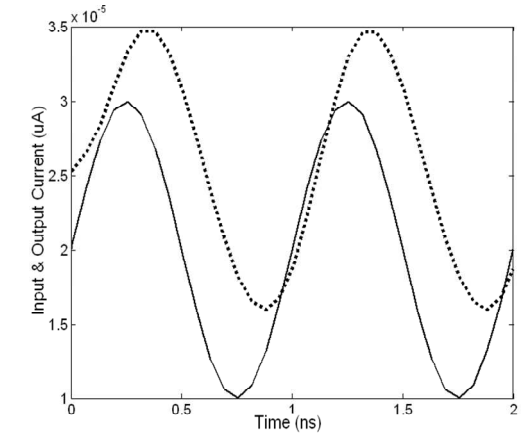

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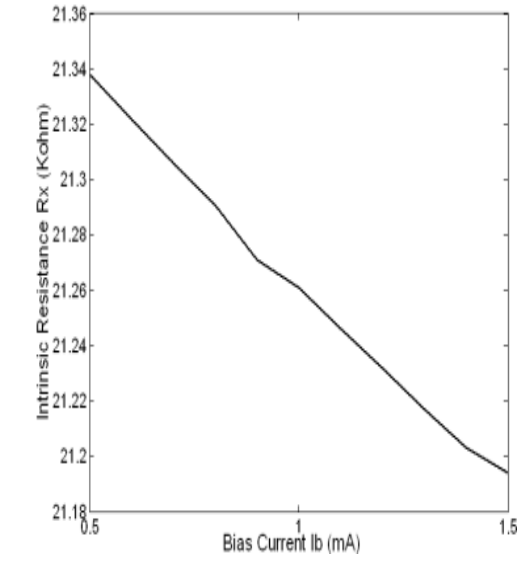

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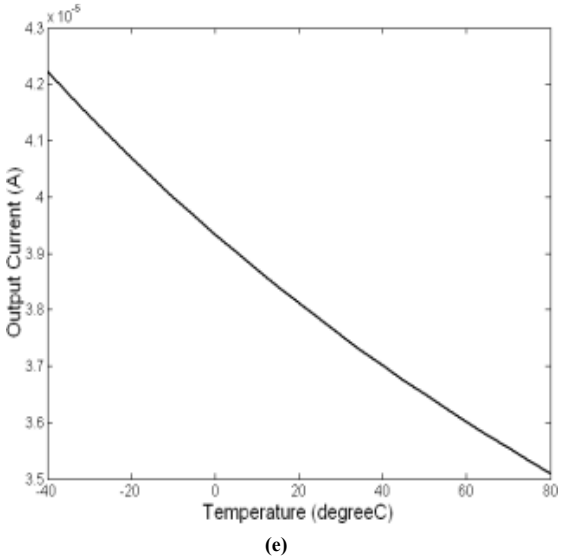


(e)

Figure 3. *Frequency Response of (a) Current Gain (Iz/Ix) (b) Voltage Gain (V_x/V_y) (c) Input signal (10uA & 800meg) and corresponding output signal (dotted curve) (d) Intrinsic resistance variation on varying bias current from 0.5mA to 1.5mA (e) Variation in output current with change in temperature from -40°C to 80°C. (about 0.0287uA/°C temperature stability).*

4. Design of Programmable CCCII

4.1. Programming Technique

To introduce programmability in basic CCCII circuit, all MOSFETs are replaced by FGMOSs. Floating-gate MOS is conventional MOSFET wherein memory is stored in the form of charge trapped on floating-gate, affecting its threshold voltage. Two antagonistic quantum mechanical transfer processes, viz. hot e- injection and Fowler Nordheim tunneling, alter the trapped charge on FG.

Table 1. *Main Characteristics of CCCII design at bias current, I_b =800μA and biasing voltage ±2v.*

AC Characteristic	
Current Gain α_0	1.079
-3db bandwidth for α_s	4.7GHz
Voltage Gain β_0	0.559
-3db bandwidth for β_s	5.24GHz
Intrinsic Resistance	26.12KΩ
Output resistance	843.56MΩ
DC Characteristic	
Offset voltage at X	35mV
Offset current at Z	350pA
Total Power dissipation	1.509mW
Temperature Stability	0.0287uA/°C

For simulation we have implemented a FGMOS model inspired from paper [16], in which the injection current and tunneling currents are modeled to program the threshold voltage of FGMOS. A schematic diagram of the FGMOS is represented in Figure 4(a) which depicts the indirect programming of FGMOS using a mos capacitor for tunneling and a programmer PMOS for injection, having common gate (the charge at this common gate can be inject/ remove thus termed as floating gate with the help of these two PMOSs). As these processes can occur during normal operation (indirect programmable FGMOS [17]), it leads additional attributes to the FGMOS transistors such as non volatile analog memory storage on floating-gate, locally computed bidirectional memory updates and memory modification during normal transistor operation. Hence the plot in Figure 4(b) illustrates the programmable threshold voltage of the FGMOS due to programmable charge at floating gate with the help of injection and tunneling mechanisms.

4.1.1. Tunneling

Charge is added to the floating gate by removing electron from it by means of Fowler-Nordheim tunneling across oxide capacitor (represented in simulation with mos capacitor). Thus, in the output characteristic of FGMOS, it shifts the curve (Figure 4(b)) to the right or in other words threshold voltage of the transistor increases.

4.1.2. Injection

Charge is removed from the floating-gate by adding electron on floating gate by impact-ionized hot electron injection from the channel to the floating gate across the thin gate oxide. Injection of electron is performed by programmer PMOS and increases charge at the common floating gate, which changes the characteristics of the FGPMOS used in respective circuit. Thus it shifts the curve (output characteristics of FGMOS in Figure 4(b)) to the left or in other words threshold voltage of the transistor decreases.

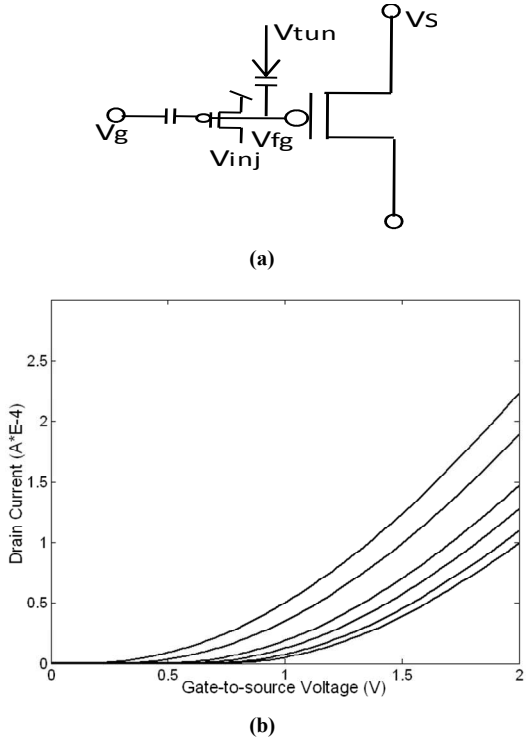


Figure 4. *(a) Pictorial representation of a FGMOS with indirectly programmable floating gate using programmer MOS for injection (Vinj = Vsource(\vdd)-Vd(\Vinj), Vinj is the pot difference between source and drain of programmer MOS) and MOS capacitor for tunneling(where V_{tun} is tunneling junction potential) (b) Output Characteristics of a FGMOS.*

4.2. Sensitivity Analysis of Specifications

Current Gain

The modified current conveyor circuit current gain and intrinsic impedance can be programmed after fabrication using a floating gate MOSFET respectively, along with offset corrections. Figure 5 represents circuit diagram of the modified CCCII where all MOSs are replaced by FGMOSs which in turn introduce programming ability of its design specifications. The current conveyor's current gain as expressed in equation (4) shows that it depends on various transistors. M12 and M13 make an identical current mirror thus the second term from equation (4) will become unity and current gain expression become:

$$A_i \cong \frac{(sC_{gd5}+g_{m5})(sC_{gd2}-g_{m2})}{(s(C_{gd5}+C_{gs5}+C_{gs4})-g_{m4})(s(C_{gs1}+C_{gs2}+C_{gd2})+g_{m1})}$$

$$\frac{I_b}{i_x}\frac{sC_{gd11}+g_{m11}}{(s(C_{gd11}+C_{gs10}+C_{g11})-g_{m10}} \quad (8)$$

In the above equation current gain depends on transconductance and after placing transconductance with respect to threshold voltages (relation shown in equation (2)), the gain shows dependence on various thresholds like, V_{t10}, V_{t11} and so on.

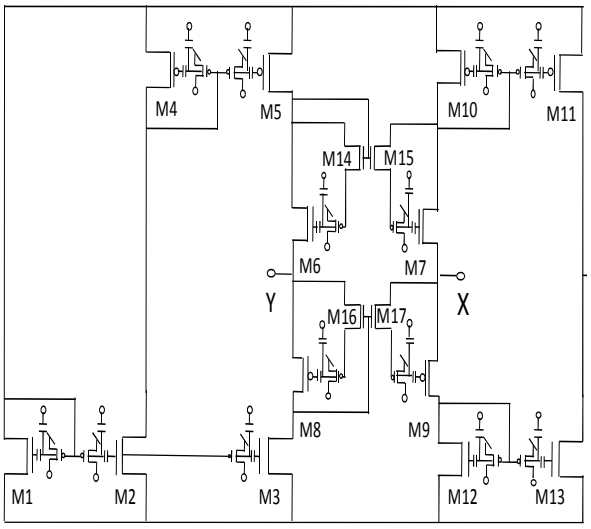


Figure 5. *Modified CCCII circuit design based on charge difference between floating-gates, simulated using BSIM3 level 49 MOSFET models in T-Spice 0.35µm CMOS process. The floating-gate transistors are being represented symbolically showing indirect, non-volatile tunneling and injection technique.*

Sensitivity of current gain with respect to threshold voltage of M10 can be evaluated by partial difference of equation (8), assuming rest all floating gate transistors with constant thresholds and hence is given by:

$$S_{Ai}/_{V_{th10}} = \frac{-k_{n10}V_{th10}}{s(C_{gd11}+C_{gs10}+C_{gd11})+k_{n10}(V_{gs10}-V_{th10})} \quad (9)$$

Neglecting the term

$$\frac{sC_{gd13}-g_{m13}}{[s(C_{gd13}+C_{gs12}+C_{gs13})+g_{m12}]},$$

as numerator is very small than denominator, sensitivity of gain with respect to $V_{th11,}$ is given by:

$$S_{Ai}/_{V_{th11}} = \frac{-k_{11}V_{th11}}{sC_{gd11}-k_{11}(V_{gs11}-V_{th11})} \quad (10)$$

The equation (9) and (10) illustrate direct dependence of gain with thresholds of transistor M10 and M11. Figure 6(a) demonstrates the respective plots.

Intrinsic Impedance: Intrinsic impedance R_x is given by

equation (1) depends on bias current I_b and transconductance of transistors M7 and M9. Substituting in terms of threshold voltage in equation (1), impedance can be expressed as:

$$R_x = \frac{1}{(k_7(V_{gs7}-V_{th7})+k_9(V_{gs9}-V_{th9})} \quad (11)$$

Sensitivity of impedance with respect to threshold of M7, assuming V_{th9} constant, is given by:

$$S_{R_x/V_{th7}} = \frac{-k_7 V_{th7}}{\left[k_7(V_{gs7}-V_{th7})+const\right]}, const = k_9(V_{gs9}-V_{th9}) \quad (12)$$

Similarly, sensitivity of intrinsic impedance with respect to V_{th9} is given by:

$$S_{R_x/V_{th7}} = \frac{-k_9 V_{th9}}{\left[k_9(V_{gs9}-V_{th9})+const\right]}, const = k_7(V_{gs7}-V_{th7}) \quad (13)$$

The plot representing sensitivity analysis of intrinsic impedance with respect to V_{t7}, as in expression (12), is shown in Figure 6 (b). The dominant floating gate transistor is M7 and hence is used for programming it after fabrication.

Output Offset Current at Z: Output offset current at Z, ($i_z(t)$) when no input signal ($i_x(t)$) is applied in the circuit, is expressed in equation (7) and in terms of thresholds, it is expressed as:

$$I_{offset} = \frac{k_2(V_{gs2}-V_{th2})k_5(V_{gs5}-V_{th5})}{k_1(V_{gs1}-V_{th1})k_4(V_{gs4}-V_{th4})}\left[\frac{k_2(V_{gs13}-V_{th13})}{k_{12}(V_{gs12}-V_{th12})} - \frac{k_2(V_{gs11}-V_{th11})}{k_2(V_{gs10}-V_{th10})}\right] \quad (14)$$

Sensitivity of offset current with respect to related thresholds, are expressed as:

$$S_{I_{offset}/V_{th2}} = \frac{-V_{th2}}{(V_{gs2}-V_{gs2})} \text{ and } S_{I_{offset}/V_{th5}} = \frac{-V_{th5}}{(V_{gs5}-V_{gs5})},$$

$$S_{I_{offset}/V_{th1}} = \frac{V_{th1}}{(V_{gs1}-V_{gs1})} \text{ and } S_{I_{offset}/V_{th4}} = \frac{V_{th4}}{(V_{gs4}-V_{gs4})} \quad (15)$$

$$S_{I_{offset}/V_{th10}} = \frac{-k_{10}V_{th10}}{\left(1/C^{-1}/k_{10}(V_{gs10}-V_{th10})\right)}, C = k_{11}(V_{gs11}-V_{th11}), \text{ assuming } g_{m13} = g_{m12} \quad (16)$$

$$S_{I_{offset}/V_{th11}} = \frac{k_{11}V_{th11}}{\left(C-k_{11}(V_{gs11}-V_{th11})\right)}, C = k_{10}(V_{gs10}-V_{th10}) \text{ assuming } g_{m13} = g_{m12}$$

$$S_{I_{offset}/V_{th12}} = \frac{k_{12}V_{th12}}{\left(C-k_{12}(V_{gs12}-V_{th12})\right)}, C = k_{13}(V_{gs13}-V_{th13}) \text{ assuming } g_{m10} = g_{m11}$$

$$S_{I_{offset}/V_{th13}} = \frac{-k_{13}V_{th13}}{(k_{13}(V_{gs13}-V_{th13})-C)}, C = k_{12}(V_{gs12}-V_{th12}) \text{ assuming } g_{m10} = g_{m11}$$

Hence offset current can be corrected using above mentioned floating gate transistors. However the dominant floating gate transistor to program offset current is M5. Therefore, gain and intrinsic impedance of modified CCCII circuit can be programmed and offset voltage and current can be corrected using a floating gate transistor respectively after fabrication.

Voltage Gain: Voltage gain between port X and Y is expressed by equation (3) while assuming transistors sizing and biasing condition constant for M6 and M7 second term of voltage gain can be neglected. Hence, voltage gain can be expressed as,

$$A_v = \frac{\left[s(C_{gs6}+C_{gs7})+k_6(V_{gs6}-V_{th6})+k_7(V_{gs7}-V_{th7})\right]}{\left[sC_{gd2}-k_2(V_{gs2}-V_{th2})\right]} \cdot \frac{\left[sC_{gd5}-k_5(V_{gs5}-V_{th5})\right]V_b/V_x}{\left[sC_{gd2}+k_2(V_{gs2}-V_{th2})\right]\left[sC_{gs7}+k_7(V_{gs7}-V_{th7})\right]} \cdot \frac{1}{\left[sC_{gd5}+k_5(V_{gs5}-V_{th5})\right]} \quad (20)$$

Sensitivity of current gain with respect to threshold voltage of M2 is given by:

$$S_{Av/V_{th2}} = \frac{\left[1-k_2(V_{gs2}-V_{th2})^2\lambda_{n2}\right]V_{th2}}{1/k_2\left[1+k_2(V_{gs2}-V_{th2})\lambda_{n2}\right]\left[1-k_2(V_{gs2}-V_{th2})\right]} \quad (21)$$

Similarly, sensitivity of voltage gain with respect to V_{th5} is

$$S_{Av/V_{th5}} = \frac{\left[k_5(V_{gs5}-V_{th5})^2\lambda_{n5}-1\right]V_{th5}}{1/k_5\left[1+k_5(V_{gs5}-V_{th5})\lambda_{n5}\right]\left[1+k_5(V_{gs5}-V_{th5})\right]} \quad (22)$$

Sensitivity of voltage gain with respect to V_{th}

$$S_{Av/V_{th6}} = \frac{-k_6V_{th6}}{[sC_{gs6}+k_6(V_{gs6}-V_{th6})+c}, c = sC_{gs7} + k_7(V_{gs7}-V_{th7}) \quad (23)$$

Similarly, with respect to V_{th7} is expressed as:

$$S_{Av/V_{th7}} = \frac{k_7V_{th7}}{[sC_{gs7}+k_7(V_{gs7}-V_{th7})][const+sC_{gs7}+k_7(V_{gs7}-V_{th7})]}, \quad (24)$$

$$const = sC_{gs6} + k_6(V_{gs6}-V_{th6})$$

The plot showing sensitivity analysis of voltage gain with respect to individual threshold voltages represented in Figure 6(c). Similarly output impedance is expressed as:

$$R_{out} = \frac{1}{\left[s(C_{gd2}+C_{gd3}+C_{gd5}+C_{gd7}+C_{gd9}+C_{gd11}+C_{gd13})+k_2(V_{gs2}-V_{th2})+k_2(V_{gs2}-V_{th2})+k_3(V_{gs3}-V_{th3})+k_5(V_{gs5}-V_{th5})+k_7(V_{gs7}-V_{th7})+k_9(V_{gs9}-V_{th9})+k_{11}(V_{gs11}-V_{th11})+k_{13}(V_{gs13}-V_{th13})\right]} \quad (25)$$

and sensitivity analysis of output resistance with respect to threshold of transistor M13 can be expressed as:

$$S_{R_{out}/V_{th13}} = \frac{-2k_{13}\lambda_{n13}(V_{gs13}-V_{th13})}{(k_{13}(V_{gs13}-V_{th13})^2\lambda_{n2}+const)} \quad (26)$$

Simulation results illustrating such programming or sensitivity of respective characteristics while considering each transistor individually will be explained by plots and programming steps along with programming range are tabulated in Table 2.

Table 2. *Programming steps to program specifications on-chip along with their range of programming.*

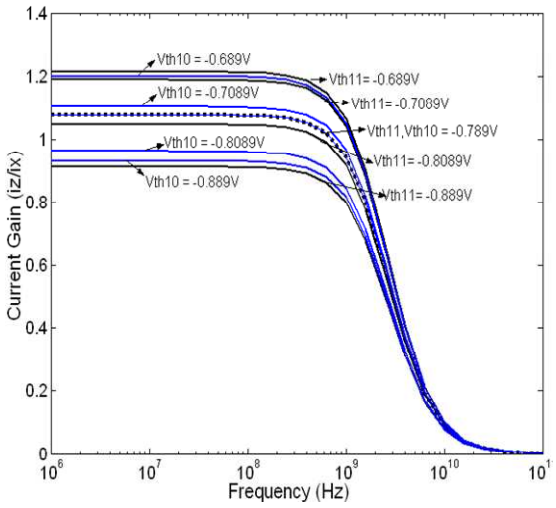
Characteristics of CCCII	Range	Programming Steps
Current Gain (A_i)	0.2 – 2.1 (can program independently with 13 bit resolution)	Program with V_{t11} while R_x , Av and Rout remain constant and offset current reduced from 261pA to 0.01pA
Intrinsic resistance (Rx)	15k – 51k (can program independently with 13 bit resolution)	Program using V_{t7} while A_i remain constant and offset current can be compensated using V_{t9}.
Voltage Gain V(X)/V(Y)	1-1.20 (cannot program it independently with accuracy)	Program using V_{t6} while R_x need to be compensation using V_{t7} and current offset correction using V_{t9}.
Output Impedance Rout (ohm*10^8)	0.5G -20G (can program independently with 13 bit resolution)	Program suing V_{t13} independently while rest all the specifications remain constant however offset current changes which can be compensated using V_{t9}
Offset current (I_z) when I_x=0 (pA)	239.40-282.34 (can be compensated independently)	Compensate using V_{t9} while rest all circuit specifications R_x, A_i, A_v and R_{out} remain constant.

4.3. Simulation Results Demonstrating Programming Steps, Used to Program Circuit Specifications

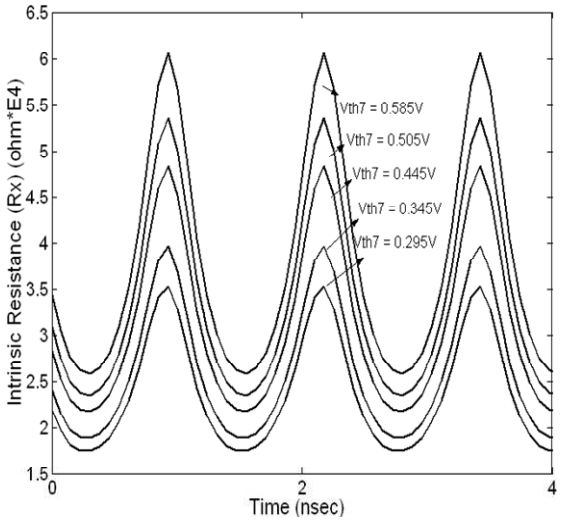
The circuit diagram of Figure 4 representing modified CCCII design is simulated using BSIM3 level 49 MOSFET models using T-Spice 0.35µm CMOS process and the final circuit with minimum number of FGMOSs is verified using Cadence analog design tool, Virtuoso. Figure 6 (a) (b) and (c) represent programmable current gain, intrinsic impedance and voltage gain with respect to threshold of floating gate transistors M11/M10, M7 and M5/M6 respectively.

Figure 7 represent parametric analysis results of specifications with respect to respective threshold model parameter, Vtho. Figure 7(a) illustrates variation of Current gain and Intrinsic Impedance and Figure 7(b) illustrate Voltage gain and Output impedance with respect to programmable thresholds of M7, Vt7. Figure 7(c) illustrates variation of offset current at Z when no input current at X with respect to Vt7. It shows that while programming Rx with Vt7, there is very less change in offset current which can be compensated using programmable Vt9(as explained in figure 7(c)). Figure 7(d) demonstrates offset current programming with respect to Vt9 respectively, while circuit specifications current gain and intrinsic impedance remain constant. Similarly Figure 7(e) and (f) represents Current gain variation and Voltage gain and Output impedance with respect to threshold of M11, Vt11. It shows while programming current gain, intrinsic impedance Rx, voltage gain Ai and output impedance Rout remain constant. However, offset current get reduced with programming Vt11, as shown in Figure 7(g). Figure 7(h) illustrate the variation in output impedance Rout with programmable threshold of transistor M13 while other specifications (current gain, voltage gain and intrinsic impedance) remain constant. Similarly voltage gain Av can be programmed using floating gate transistor M6; however, while programming Av, intrinsic impedance Rx also varies. Thus, for independent programming of voltage gain, variation in intrinsic impedance needs to be compensated using floating gate transistor M7. Hence the modified programmable CCCII demonstrate independently programmable current gain using Vt11 and independently programmable intrinsic impedance i.e. programmable current control using Vt7, while offset current can be compensated using Vt9. In addition to, it can program voltage gain with programmable threshold Vt6 along with little compensation of other specifications (Rx compensation using Vt7 and offset current compensation using Vt9) and independent programming of output impedance with programmable threshold Vt13. The Table 2 demonstrates the design data sheet illustrating the complete programming steps to program each specification

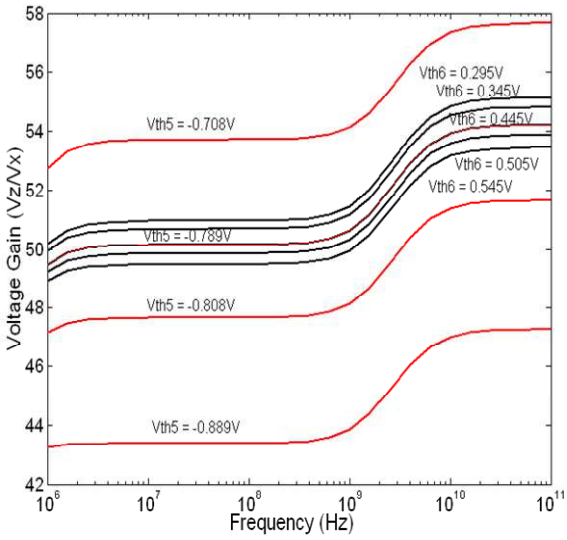
independently and with 13-bit resolution accuracy. For particular sizing and biasing condition of the circuit it represent the programming range of each specification. It shows for particular sizing and biasing condition current gain can be programmed within 0.2 to 2.1 values with 13-bit programming resolution using a FGMOS M11 while offset current reduces from 261pA to 0.01pA. Intrinsic impedance can be programmed between the range from 15K to 51K using a FGMOS M7 while offset current can be compensated using FGMOS M9. However voltage gain can be programmed using M6 while intrinsic impedance need to be compensated using M7 and offset current using Vt9. In addition to output impedance is programmable within the range from 0.5Gohm to 20Gohm using a FGMOS M13, where all other specifications remain constant but offset current vary which can be compensated using M9. And offset current at Z when no input current is applied can be program independently using FGMOS M9. After sensitivity analysis using model parameter Vtho analysis, floating gate transistor simulation model (influenced from paper [17]) using external voltage sources Vtun, for tunneling and Vinj for injection is placed and simulation results are incorporated in Figure 7. It demonstrates current gain variation with variable tunneling voltage in Figure 8(a). The continuous variation in current gain with programmable injection of change at floating gate with the help of variable drain voltage (Vd_prog) of the programmer PMOS voltage is illustrated in Figure 8(b). Moreover Figure 8(c) demonstrates intrinsic resistance variation with programmable charge at floating gate with variable tunneling voltage and with programmable intrinsic resistance using injection is shown in Figure 8(d). Thus, the final modified circuit consists of three floating gate transistors is illustrated along with its fabrication layout in Figure 9.



(a)

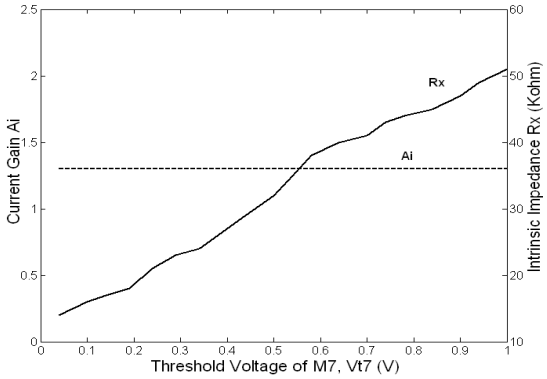


(b)

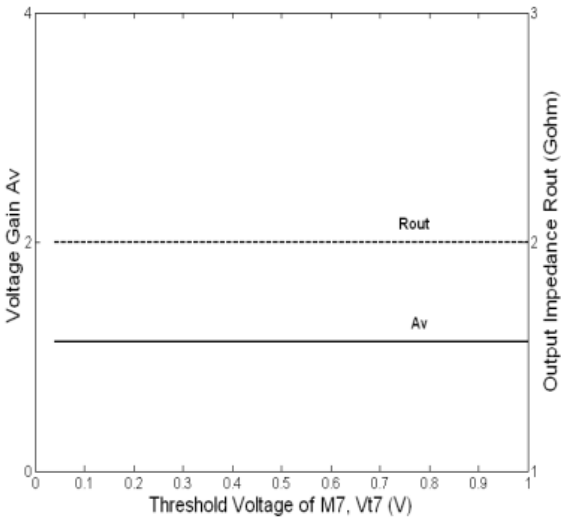


(c)

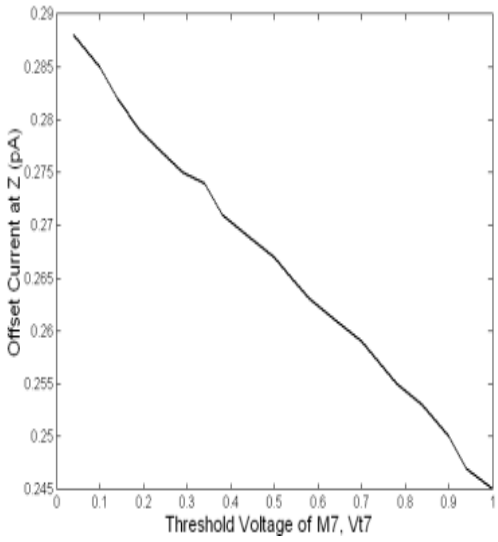
Figure 6. *(a) Variation of Current gain with programmable thresholds of M10&M11 floating-gate transistors (b) Variation of intrinsic impedance Rx with programmable threshold of M7 floating-gate transistors (c) Variation of Voltage gain Av with programmable threshold of M5 &M6 floating-gate transistors.*



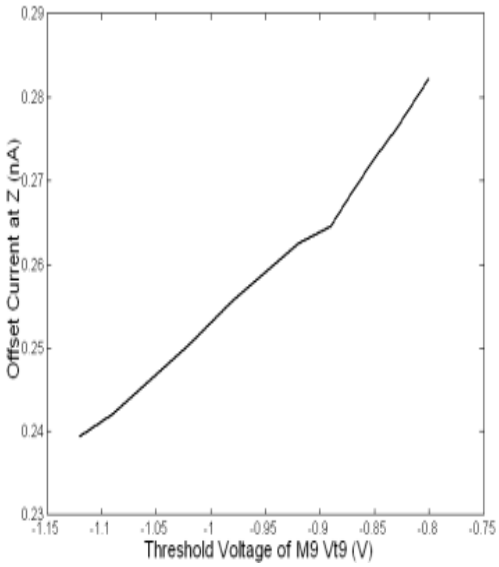
(a)


Voltage Gain Av
Output Impedance Rout (Gohm)
Rout
Av
Threshold Voltage of M7, Vt7 (V)

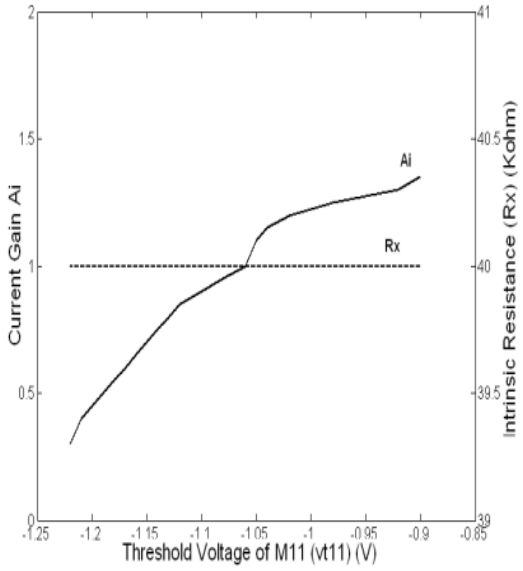
(b)


Offset Current at Z (pA)
Threshold Voltage of M7, Vt7

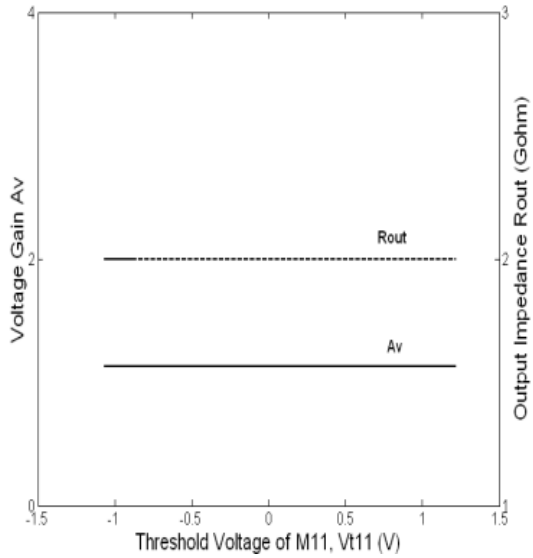
(c)


Offset Current at Z (nA)
Threshold Voltage of M9 Vt9 (V)

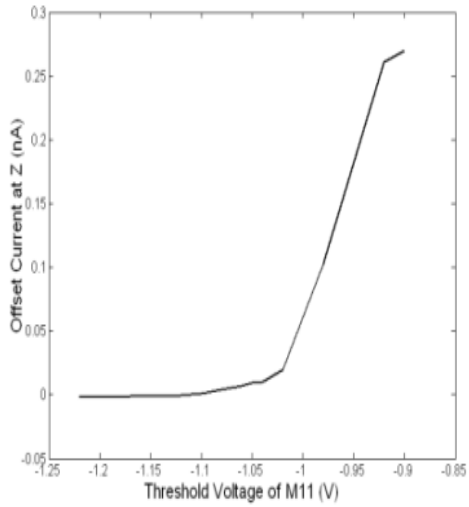
(d)


Current Gain Ai
Intrinsic Resistance (Rx) (Kohm)
Ai
Rx
Threshold Voltage of M11 (vt11) (V)

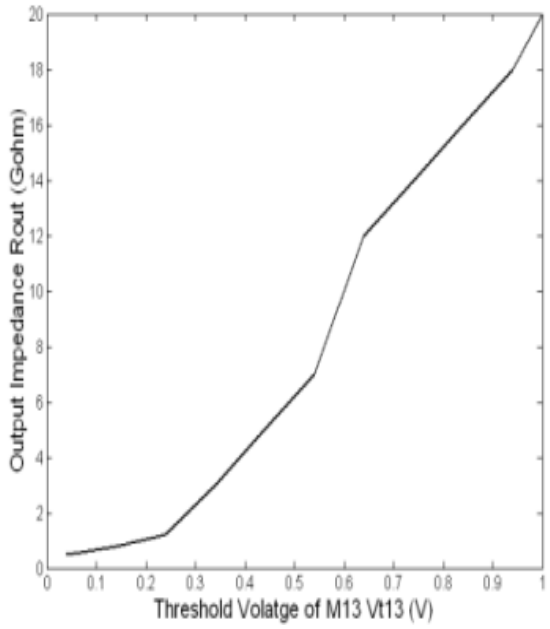
(e)


Voltage Gain Av
Output Impedance Rout (Gohm)
Rout
Av
Threshold Voltage of M11, Vt11 (V)

(f)

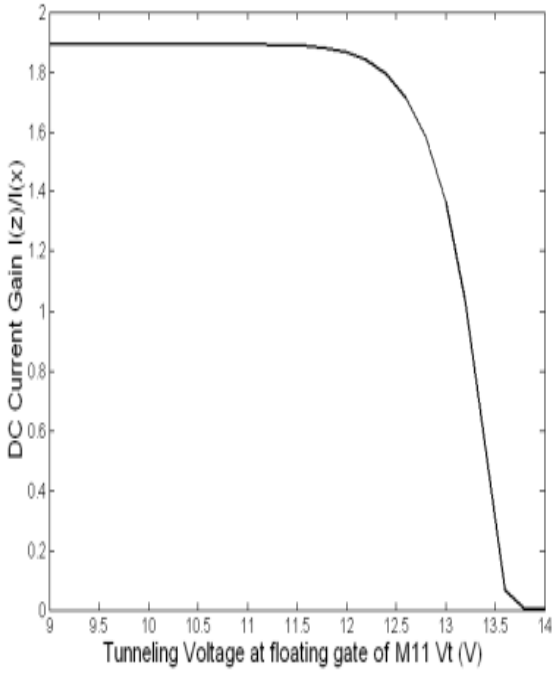

Offset Current at Z (nA)
Threshold Voltage of M11 (V)

(g)

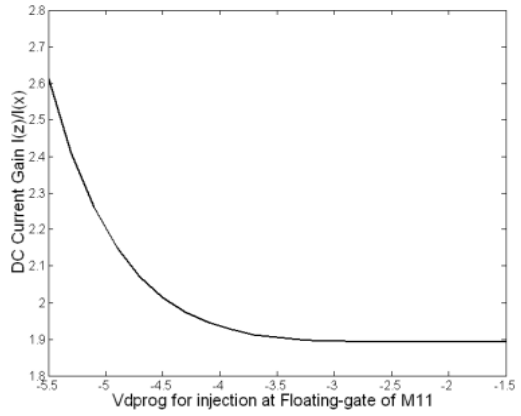


(h)

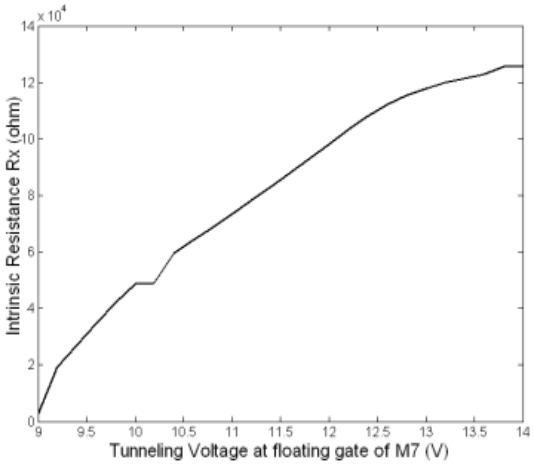
Figure 7. *(a) Variation of Current gain and Intrinsic Impedance with programmable thresholds of M7, Vt7 (b) Variation of Voltage gain and Output Impedance with programmable thresholds of M7, Vt7 (c) Variation of offset current at Z when no input current w.r.t Vt7 (shows while programming Rx with Vt7, very less change in offset which can be compensated with vt5) (d) Variation of offset current at Z w.r.t Vt5 (e) Variation of Current gain and Intrinsic Impedance with programmable thresholds of M11(f) Variation of Voltage gain and Output Impedance with programmable thresholds of M11, Vt11 (g) Variation of offset current at Z when no input current at X w.r.t Vt11(demonstrate that the offset current decreases while programming current gain or with increase in Vt11, offset decreases) (h) Variation of Output impedance Rout with programmable thresholds of M13 while rest all specifications current gain Ai, Intrinsic impedance Rx and voltage gain Av remain constant.*



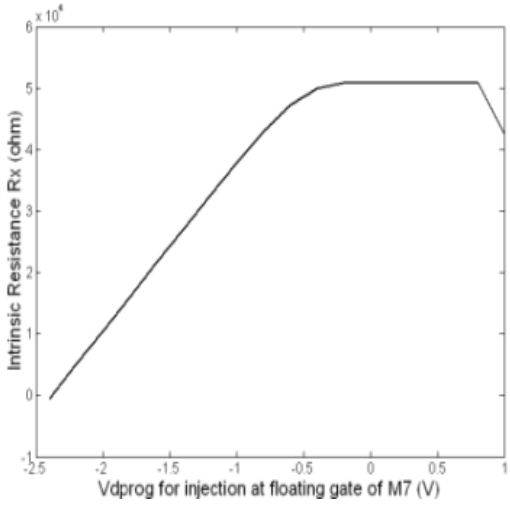
(a)



(b)



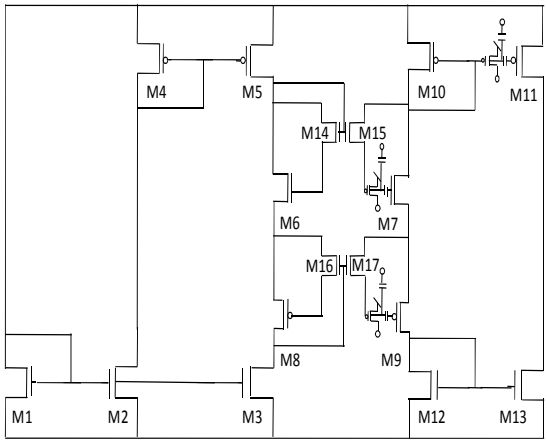
(c)



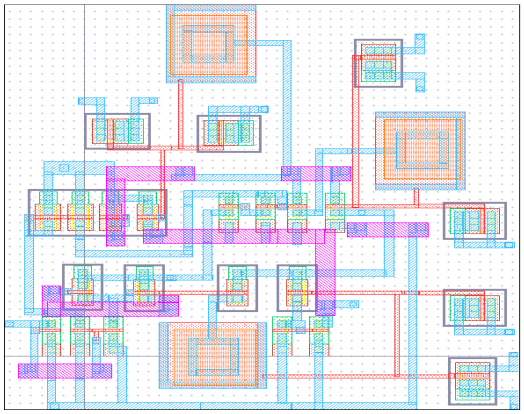
(d)

Figure 8. *(a) Variation in dc Current Gain with tunneling voltage Vt, variation at the floating gate of floating gate transistor M11. (b) Variation in dc Current Gain with drain voltage of programmable FET, Vdprog, variation at common floating gate (however, injection voltage, Vinj= Vsprog-Vdprog), of floating gate transistor M11 (c) Variation in Intrinsic Impedance with tunneling voltage Vt, at the floating gate of floating gate transistor M7 (d) Variation in Intrinsic Impedance with drain voltage of programmable FET, Vdprog, variation at common floating gate (however, injection voltage, Vinj= Vsprog-Vdprog), of floating gate transistor M11).*

4.4. Final CCCII Circuit with Required Floating Gate Transistors and Its Programming Steps



(a)



(b)

Figure 9. *(a) Schematic of final modified Field Programmable CCCII developed using BSIM 3 level 49 models from the MOSIS fabrication services, in Virtuoso (Cadence analog designer tool) 0.35µm CMOS process using three FGMOSs. (b) Layout of final CCCII circuit in which gain and impedance can be programmed independently using a floating gate transistor (M11 and M7 respectively), which in turn can be programmed using two PMOSs (mos capacitor for tunneling and programmer PMOS for injection) at common floating gate, using external control voltages V_{tun} and V_{inj}, whereas, the charge at the floating gate can be stored at capacitor (160pF), placed between gate and floating gate of the floating gate transistor. The circuit occupies 65µm × 54µ chip area.*

The final modified programmable CCCII circuit which has independently accurate programmable current gain and current control along with offset current compensation is developed using only three floating gate transistors M11, M7 and M9 using Virtuoso, as shown in Figure 9(a). The modified circuit consists of FGMOSFET synapse model [24] which has input capacitor of value 160fF between gate and floating gate and two programmable pFETs with common floating gate, used for tunneling (using terminal vtun for example vtunforM11) and injection (using terminal vd_prog and vs_prog for example vdprogforM11/vsprogforM11)of charges at the floating gate. The design is also being developed for fabrication and the layout is demonstrated in Figure9 (b). The circuit occupies 65µm × 54µ chip area. The layout too represents the modified CCCII circuit with three FGMOSFETs M11, M7 and M9. Each FGMOSFET consists of an input storing capacitor and two programming pFETs.

5. Conclusion

The proposed programmable CCCII design and final modified CCCII design simulation results illustrate that the circuit specifications, current gain, intrinsic impedance, voltage gain and output impedance can be programmed using floating gate transistor M11, M7, M6, M13 while offset current can be compensated using M9. The circuit specifications of modified second generation current conveyor are programmable after fabrication to desired value in the specific range using respective floating gate transistors as expressed in form of programming steps. And the specifications can be programmed with 13bit programming precision. As we have observed that specifications like current gain is programmable to very fine values, i.e. up to 13 bit precision and the same were claimed in paper [25] with experimental verification as well. Thus our proposed design can be programmed by field user continuously. Hence all three design objectives; variation in the specifications should be large and continuous, variation of each specification should be independent of the other and the operating point of the circuit should not alter too much during programming, i.e. offset current should not vary significantly, have been justified from our results. Therefore, proposed current conveyor design with fine programming of its design specifications after fabrication, occupy smaller chip area, low power consumption, show thermal stability and simpler procedure of on-chip programming. Thus it can be used to implement universal filter with fine-tunable central frequency and can be used as oscillator with fine tunable oscillating frequency. It can also be used to develop field programmable analog arrays where no additional circuitry is required for analog storing (non-volatile, indirect field-programming ability feature of FGMOS), to program its FGMOS analog voltages are used, hence for interconnections no extra circuitry will be required. Moreover the applicability of this design can be extended to remote electronic systems (like in electronic circuitry of spacecrafts) as well as in portable devices (as analog, compact hardware used).

Acknowledgment

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