

Pulse Bursting Phenomenon in Constant On-time Controlled Boost Converter

Song Wei¹, Li Shaopeng²

¹China Railway International CO. LTD., Beijing, China

²China Railway Design Corporation, Tianjin, China

Email address:

songwei@cric.rs (Song Wei), liseanh@163.com (Li Shaopeng)

To cite this article:

Song Wei, Li Shaopeng. Pulse Bursting Phenomenon in Constant On-time Controlled Boost Converter. *American Journal of Traffic and Transportation Engineering*. Vol. 7, No. 1, 2022, pp. 14-18. doi: 10.11648/j.ajtte.20220701.12

Received: December 21, 2021; **Accepted:** January 14, 2022; **Published:** January 21, 2022

Abstract: Constant on-time (COT) is a pulse frequency modulation based control method, which is widely used for the controller of switching mode power supplies due to the advantages of simple implementation, low cost and good performances. In fact, like hysteretic control, COT is also a ripple-based control, and its loop stability is very dependent on the output voltage ripple characteristic. COT controlled buck converter is mainly concerned in nowadays. For boost converter, the output voltage ripple characteristic is quite different with that of buck converter. Thus, the stability of COT controlled boost converter is necessary to be investigated. In this paper, with particular theoretical analysis, the unique pulse bursting phenomenon in COT controlled boost converter appears when the time constant of the output capacitor is relatively small, which results in large inductor current and output voltage swing. The quantitative relationship between the time constant and the other circuit parameters such as input voltage, output current and inductance is deduced, which is very different with that of COT controlled buck converter. Simulation and ex-perimental results are provided to verify the theoretical analysis results. The investigation presented in this paper gives an im-portant guideline for the circuit parameter design of COT con-trolled boost converter.

Keywords: Pulse Bursting, Constant On-time (COT), Boost Converter, Time Constant

1. Introduction

Constant On-time (COT) control technique has been widely used to the control of switching dc-dc converter in recent years, and it has attractive advantages such as simple implementation, simple control loop design and low cost [1-8]. In addition, it not only has high conversion efficiency under light load, but also has the advantage of fast input voltage and load transient response. In addition, it is worth noting that the absence of error amplifiers and their corresponding compensation networks results in converters that easily have a higher control loop gain bandwidth and remain stable over a wider range of input voltage or load variations.

Up to now, nearly all the efforts about COT control are developed based on buck converter. In literature [9], the pulse bursting phenomenon in COT controlled buck converter is revealed, which is somewhat similar to what will be presented in this paper. As we all know, the boost converter and the buck converter are two dual circuits, and they have different characteristics. Therefore, in order to give an overall

evaluation of COT control, it is necessary to analysis its performances in boost converter.

This paper reveals the pulse burst phenomenon of the COT-controlled boost converter and analyzes the effect of the time constant of the output capacitor on this phenomenon. While pulse bursting phenomenon occurs, large inductor current and output voltage variation in steady state are presented, which deteriorates the performances of the boost converter. The quantitative relationship between the time constant and the other circuit parameters such as input voltage, output current and inductance is deduced, and the critical time constant is obtained. While the output capacitor's time constant is less than the critical value, the pulse bursting phenomenon occurs. On the other hand, while the time constant is higher than the critical value, the bursting phenomenon disappears. In order to verify the theoretical analysis, simulation and experimental results are provided in this paper. The analysis results presented in this paper help the designer optimize circuit parameters while applying COT control to boost converter.

2. Pulse Bursting Phenomenon

2.1. Review of Boost Converter with COT Control

The circuit block diagram of the COT-controlled boost converter and its main operating waveforms are referred to Figure 1, where RESR represents the equivalent series resistance (ESR) of the output capacitor. As we know, for boost converter, if the power switch is on, the output voltage decreases. Thus, it must limit the maximum duty cycle of the control pulse to avoid the power switch always on in startup or transient process. Therefore, in COT controlled boost converter, it needs an additional off-time module to make the power switch off for a very short time after the constant

on-time duration, to get the inductor away from saturation in startup or transient process. That's the main difference with the COT controller applied in buck converter [9].

The operation principle can be referred to Figure 1(b). While the power switch S is on during the constant on-time duration, the inductor current i_L increases and the output voltage V_o decreases. Once the constant on-time T_{ON} is over, the off-time module is active, which makes the reset signal maintain high level to turn off S for duration of T_{off_min} . When minimum off-time T_{off_min} is over, if V_o is lower than the reference voltage V_{ref} at this time, S is turned on again and the next switching cycle begins; on the other hand, if V_o is higher than the reference voltage V_{ref} , S keeps off until V_o drops below V_{ref} .

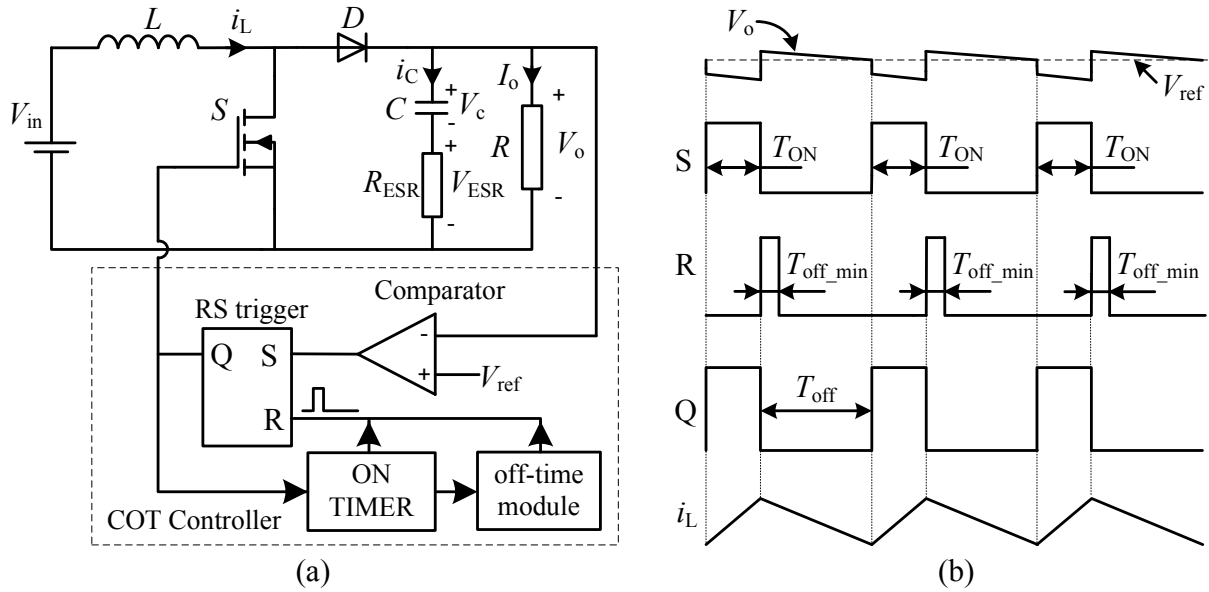


Figure 1. COT controlled boost converter: (a) circuit block diagram, and (b) main operation waveforms.

2.2. Pulse Bursting Phenomenon Analysis

In order to analyze the pulse bursting phenomenon in COT controlled boost converter, it is necessary to investigate the output voltage ripple [10].

It is known that the overall output voltage ripple is composed of two terms, v_c and v_{ESR} [11]. Where v_c is capacitor-based voltage ripple, which depends on the value of i_L and I_o , and v_{ESR} is ESR-related voltage ripple, which is proportional to the value of R_{ESR} . Generally speaking, the inductor current i_L is usually larger than the load current I_o for boost converter [12]. Thus, when S is turned on, the output capacitor provides energy to the load that makes v_c decrease [12]; on the other hand, when S is turned off, v_c increases due to $i_L > I_o$ [10-13].

Without loss of generality, we can assume the value of R_{ESR} is too small to dominate the overall output voltage ripple [13]. For qualitative analysis, the extreme case $R_{ESR} = 0$ can be considered. In this situation, while S is turned off, V_o keeps on increasing until i_L drops below than I_o . While $i_L < I_o$, V_o decreases. The next switching cycle begins until V_o drops below than V_{ref} . At the moment while V_o is just below than V_{ref} ,

it can be assumed that i_L is much lower than I_o , even it descends to zero in worse case. Then S is turned on for T_{ON} and i_L increases. The output capacitor provides energy to the load, that makes V_o still decrease. While S is turned off, i_L flows into the load side, but the output voltage usually can not be regulated to larger than V_{ref} within T_{off_min} . S is thus turned on again and i_L keeps on increasing. This case will go on until i_L is large enough to make V_o larger than V_{ref} within T_{off_min} . In this way, after a few periods of T_{ON} and T_{off_min} in series, S is turned off for quite a long time, which causes large inductor current and output voltage swing, i.e. [13] the so-called pulse bursting phenomenon occurs. The description above can be referred to Figure 2.

However, while the value of R_{ESR} is large enough to dominate the output voltage ripple, the control case should be quite different. In this situation, when S is turned off, V_o decreases immediately rather than requiring $i_L < I_o$ as the case described before, and the waveforms as shown in Figure 1 appears. Therefore, pulse bursting phenomenon will not occur, and the COT controlled boost converter operates in normal with small inductor current and output voltage variation [13].

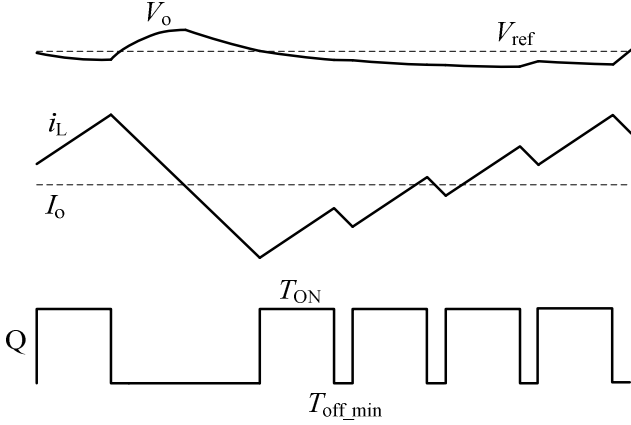


Figure 2. Pulse bursting phenomenon in COT controlled boost converter.

2.3. Critical ESR for Pulse Bursting Phenomenon

From the analysis above, it can be seen that large value of R_{ESR} can efficiently suppress inductor current and output voltage swing, but which will result in large output voltage ripple [13]. Thus, it is wise to choose appropriate value of R_{ESR} . In order to evaluate how large R_{ESR} is enough, it is necessary to obtain the ratio of voltage ripple between v_c and v_{ESR} while S is turned off in steady state [14, 15].

In steady state while S is turned off in a switching cycle, the variation of capacitor-based voltage ripple ΔV_c can be expressed as

$$\Delta V_c = \frac{\Delta Q}{C} = \frac{I_o T_{ON}}{C} \quad (1)$$

and the variation of ESR-related voltage ripple ΔV_{ESR} can be obtained as

$$\Delta V_{ESR} = \Delta i_L R_{ESR} = \frac{V_{in}}{L} T_{ON} R_{ESR} \quad (2)$$

So, the ratio can be written as

$$\frac{\Delta V_c}{\Delta V_{ESR}} = \frac{I_o L}{V_{in} R_{ESR} C} \quad (3)$$

In order to make ΔV_{ESR} dominate the output voltage ripple, the ratio must be less than one, thus we have

$$R_{ESR} \geq \frac{I_o L}{V_{in} C} \quad (4)$$

i.e. the critical ESR is gotten. To ensure normal operation, the value of R_{ESR} should be larger than that. Otherwise, pulse bursting phenomenon will occur [14].

From (4), it can be seen that the time constant τ of output capacitor must be designed to satisfy with following [14]

$$\tau = R_{ESR} C \geq \frac{I_o L}{V_{in}} \quad (5)$$

which only with respect to the main circuit parameters of boost converter. That is quite different with that of COT controlled buck converter, in which only the control parameter of T_{ON} is relative [9].

3. Simulation and Experimental Results

In this section, simulation and experimental results are provided to verify the theoretical analysis, with the circuit parameters as follows: $V_{in}=5V$, $V_o=20V$, $L=200\mu H$, $C=470\mu F$, $T_{ON}=7.5\mu s$, $T_{off_min}=0.5\mu s$.

Figure 3 shows $v_o(nT)$ as functions of R_{ESR} and I_o by using discrete mapping iterative model [9], where $v_o(nT)$ stands for the steady state output voltage at the beginning of the n -th switching cycle, and in Figure 3(a) I_o is 0.5A, R_{ESR} is 42.5mΩ in Figure 3(b). From Figure 3(a), it can be seen that when R_{ESR} is smaller than 42.4mΩ, $v_o(nT)$ is always less than or equal to the desired voltage 20V, i.e. the pulse bursting phenomenon occurs. While R_{ESR} is larger than 42.4mΩ, the pulse bursting phenomenon vanishes and the COT controlled boost converter operates normally, with $v_o(nT)$ be regulated at 20V. Thus, $R_{ESR}=42.4m\Omega$ is the critical ESR, which is quite close to 42.5mΩ as obtained from (4), and the difference is caused by simulation precision. Similarly in Figure 3(b), it can be seen that while I_o is less than 0.506A, the COT controlled boost converter operates normally and no pulse bursting phenomenon occurs, which is also well verified the theoretical analysis in (4).

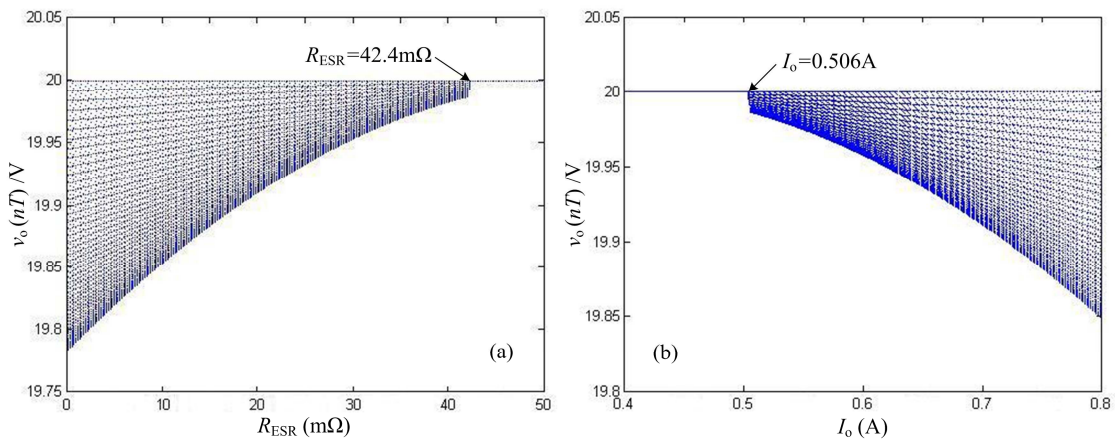


Figure 3. $v_o(nT)$ as functions of R_{ESR} and I_o : (a) R_{ESR} (b) I_o .

Although only parameters of R_{ESR} and I_o are chosen to illustrate the effect on pulse bursting phenomenon, the effect of other parameters (like V_{in} , C , L) can also be performed, and it is always found that the conclusion drawn in (4) is valid. So, only the effect of R_{ESR} is presented in the following paragraphs.

Figures 4(a) and (b) show the simulation results of COT controlled boost converter with $R_{ESR} = 35m\Omega$ and $R_{ESR} = 56m\Omega$ while $I_o = 0.5A$, where V_{GS} stands for the control

pulse. In Figure 4(a), it can be seen that S is turned on consecutively for a bunch of constant on-time intervals, and then turned off for a relatively long time [9]. In this case, the so-called pulse bursting phenomenon occurs, which results in obviously large output voltage and inductor current variation. However, as shown in Figure 4(b), when $R_{ESR} = 56m\Omega$, the COT controlled boost converter operates normally with much smaller output voltage and inductor current ripples [16].

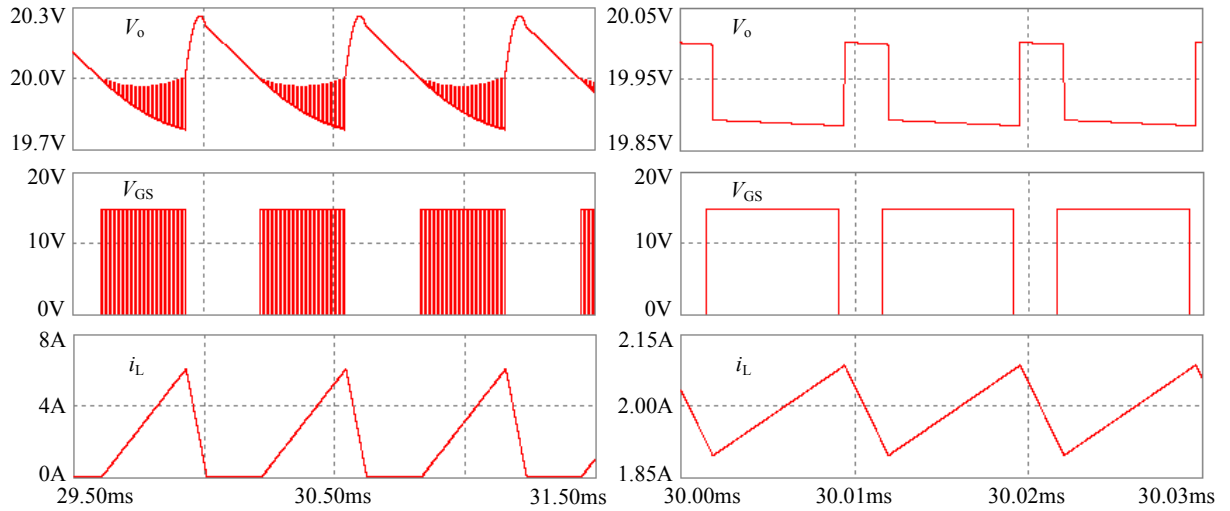


Figure 4. Simulation results of COT controlled boost converter: (a) $R_{ESR} = 35m\Omega$, and (b) $R_{ESR} = 56m\Omega$.

Figure 5 presents the corresponding experimental results of COT controlled boost converter, where ΔV_o stands for output voltage ripple and V_{GS} stands for the control pulse [12].

Similar to simulation results, while $R_{ESR} = 35m\Omega$, pulse bursting phenomenon occurs and it disappears while $R_{ESR} = 56m\Omega$. Experimental results well verify the simulation results.

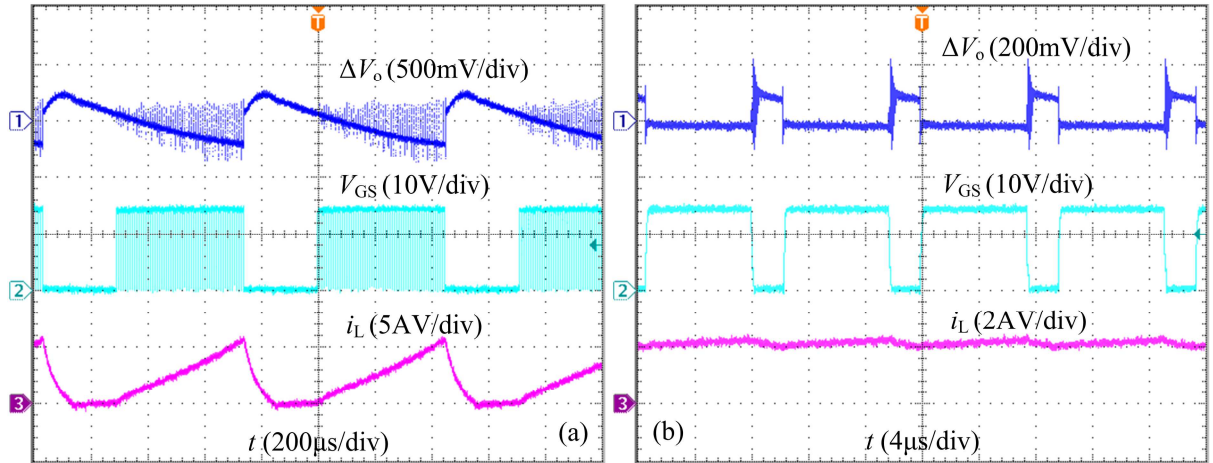


Figure 5. Experimental results of COT controlled boost converter: (a) $R_{ESR} = 35m\Omega$, and (b) $R_{ESR} = 56m\Omega$.

4. Conclusion

In this paper, pulse bursts occur in the COT-controlled boost converter when the time constant of the output capacitor is relatively small, which leads to large variations in the inductor current and output voltage at steady state, but the characteristics of the output voltage do not violate the COT control. In order to

suppress pulse bursting phenomenon, the output capacitor's time constant as functions of the other main circuit parameters is deduced, and it is independent of the key control parameter like T_{ON} . The findings of this paper are useful for the design of the main circuit parameters of COT-controlled boost converters, for example, to avoid pulse bursts throughout the operating range, the time constant of the output capacitor should be chosen considering the maximum load current.

References

- [1] S.-S. Hong and B. Choi, "Technique for developing averaged duty ratio model for DC-DC converters employing constant on-time control," *Electronics Letters*, vol. 36, no. 5, pp. 397-399, Mar. 2000.
- [2] Li, D., S. C. Wong, and K. T. Chi. "Bifurcation Analysis of a Current-Mode Controlled DC Cascaded System and Applications to Design." *IEEE Journal of Emerging and Selected Topics in Power Electronics* PP. 99 (2020): 1-1.
- [3] N. Kong, D. S. Ha, J. Li, and F. C. Lee, "Off-time prediction in digital constant on-time modulation for dc-dc converters," in *Proc. IEEE Int. Symp. Circuits Syst*, 2008, pp. 3270-3273.
- [4] Aroudi, A. E., et al. "Analytical Determination of Fast-Scale Instability Boundaries for Current Mode Controlled DC-DC Converters With CPL and Closed Voltage Loop." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 11. 1 (2021): 39-48.
- [5] Ridley, R. B.. "A new, continuous-time model for current-mode control." *IEEE Transactions on Power Electronics* 6. 2 (1991): 271-280.
- [6] X. Xu and X. Wu, "High dimming ratio LED driver with fast transient boost converter," in *Proc. IEEE PESC*, 2008, pp. 4192-4195.
- [7] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218-1230, May. 2010.
- [8] Chanrong, et al. "A high performance adaptive on-time controlled valley-current-mode DC-DC buck converter." *Journal of Semiconductors* v. 41. 06 (2020): 53-60.
- [9] J. Wang, J. Xu, and B. Bao, "Analysis of pulse bursting phenomenon in constant-on-time-controlled buck converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5406-5410, Dec. 2011.
- [10] Cho, Younghoon, and P. Jang. "Analysis and Design for Output Voltage Regulation in Constant-on-Time-Controlled Fly-Buck Converter." *Electronics* 10. 16 (2021): 1886.
- [11] Michal, V., Z Nicolò, and A. Matteo. "Low-complexity inductance estimation for switched-mode power converters using peak-current mode control." *IET Power Electronics* 13. 11 (2020): 2269-2273.
- [12] Liu, K. P., et al. "Control circuit and method for a constant on-time PWM switching converter." US, US20080030181 A1. 2010.
- [13] Morong, W. H., and T. E. Lawson. "Power converter with demand pulse isolation." (2015).
- [14] Yen, Tzu Yang, and C. Y. Chen. "Constant-on-time generation circuit and buck converter." (2014).
- [15] M. D. Bermardo and F. Vasca, "Discrete-time maps for the analysis of bifurcations and chaos in DC/DC converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 2, pp. 130-143, Feb. 2000.
- [16] Wang, J., et al. "Dynamical Effects of Equivalent Series Resistance of Output Capacitor in Constant On-Time Controlled Buck Converter." *IEEE Transactions on Industrial Electronics* 60. 5 (2013): 1759-1768.