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Phonon Effect with Short Drain and Source in Nanowires DGMOSFET SI

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Abstract: Temperature dependence of the drain current of a MOSFET plays a crucial role in the device performance and power dissipation has become a major obstacle in performance scaling of modern integrated circuits, and has spurred the search for devices operating at lower voltage swing. In this paper, we propose the application of a symmetric Double Gate (SDG) in a Tunnel Field Effect Transistor (TFET) to simultaneously optimize the on-current, the off-current and the threshold voltage, and also improve the average subthreshold slope, the nature of the output characteristics and the immunity against the DIBL effects. We demonstrate that if appropriate work-functions are chosen for the gate materials on the source side and the drain side, the tunnel field effect transistor shows a significantly improved performance. We apply the technique of SDG in a Strained Double Gate Tunnel Field Effect Transistor with an Oxide gate dielectric to show an overall improvement in the characteristics of the device along with achieving a good on-current and an excellent average subthreshold slope. The results show that the SDG technique can be applied to TFETs with different channel materials, channel lengths, gate-oxide materials, gate-oxide thicknesses and power supply levels to achieve significant gains in the overall device characteristics. The on-current of these devices is mainly limited by the tunneling barrier properties, and phonon scattering has only a moderate effect.

Keywords: Variability, Microelectronics, Silicon, Nanowire, NEGF, MOSFET, Phonon

1. Introduction

Short-Channel Effects (SCEs) and series source/drain resistance are great challenges in the migration of processing technology to deep sub-100nm regime.

Ultra thin body (UTB) multi-gates MOSFET with source/drain engineering is suggested [11] as an emerging technology to be studied by the International Technology Roadmap for Semiconductors (ITRS) [5].

SCEs has made the scaling of conventional MOSFET structure difficult. As the channel potential of the MOSFET is controlled by all the terminals, drain controllability will increase and gate controllability will decrease when the channel length (L) is scaled down, which will intensify the SCEs [6]. The SCEs may cause large off-current through drain induced barrier low (DIBL) effect. When the SCEs are serious, the drain can turn on the channel even if the gate is biased in the off region, which is so-called “punch-through”.

Reducing the gate oxide thickness and increasing the doping concentration used to be the conventional solutions for SCEs control in the past generations [3]. Reducing the gate oxide thickness will directly increase the gate to channel coupling ratio while increasing the doping concentration can reduce off-current and prevent “punch-through”.

However, these methods are becoming less effective for two main reasons. Firstly, the equivalent oxide thickness (EOT) of the gate oxide-nitride layer nowadays is less than 1.2nm, which is as thick as only a few atom layers [2]. Further scaling the EOT of the gate dielectric will cause large gate leakage current [1]. Secondly, increasing doping concentration will cause many side effects such as doping fluctuation, lower mobility and higher Source/Drain

capacitance [7]. As the degree of doping fluctuations increases at small dimensions, the threshold voltage (VT) variations will be unacceptable for circuit applications if high doping concentration is employed. According to the gate and channel numbers, Multi-Gate structures can be divided into Double gate (DG), Tri-Gate, Pi-Gate and Quadruple-Gate structure [4].

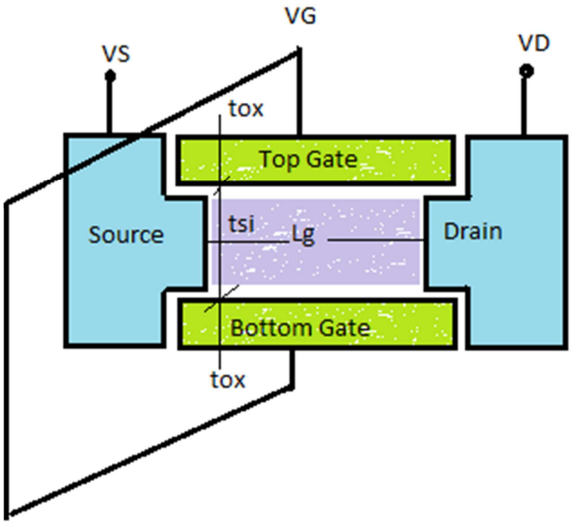

Figure 1. *Structure of double gate and Electric field lines originating from the drain for DG MOSFET. IN DGMOSFET, in contrast, lines are terminated on either top or bottom gate.*

Although the DG MOSFET is easier to be scaled down, it is much difficult to fabricate a gate under single crystal channel. Selective Epitaxial with Lateral Over-growth (SELO) is an example for planar DG fabrication [13].

Due to the great challenges facing the scalability of bulk MOSFETs, industrial and academic efforts are now being exerted to find a replacement [12]. There are two main directions, adopting new transistor structures or adopting new materials. New transistor structures seek to improve the electrostatics of the MOSFET (i.e. to increase the gate voltage control on the transistor) to reduce the SCEs [10]. Among these structures is the Double-Gate (DG) MOSFET. The DG FET shown in Figure 1 was proposed in 1984 [8]. It was shown that one can improve the immunity to SCEs using a top as well as a bottom gate. The usage of two gates, instead of one, showed excellent gate control on the channel potential [9]. Moreover, the usage of two gates increase the device current capability due to larger gate capacitance per unit area.

In contrast, when another gate is added at the bottom, as shown in Figure 1, the electric field lines will properly be terminated at either the top or bottom gate. Thus the drain control on the channel potential is reduced leading to more immunity to DIBL.

Phonon Dispersion Model

The present work treats all phonon scattering events inelastically, hence the electrons exchange the correct amount of energy (corresponding to the absorption or emission of a phonon) with each scattering event [1]. Particular attention is paid to the treatment of inelastic acoustic phonon scattering, to properly account for energy dissipation at low temperatures and low electric fields. Treating the acoustic phonons inelastically is also important for heat generation spectrum calculations [13].

As in the traditional analytic-band approach, scattering with six types of intervalley phonons is incorporated. Intervalley scattering can be of g-type, when electrons scatter between valleys on the same axis, e.g. from <100>to <−100>, or of f-type when the scattering occurs between valleys on perpendicular axes, e.g. from <100>to <010> [5]. The phonons involved in these scattering transitions (three of f-type and three of g-type) can be determined from geometrical argumentsand are labeled in Figure 5.

Intravalley scattering refers to scattering within the same conduction band valley and usually involves only acoustic phonons [8].

Most typical NEGF codes, both analytic- and full-band, treat intravalley scattering with a single kind of acoustic phonon. This simplification is accomplished by grouping the longitudinal acoustic (LA) and transverse acoustic (TA) branches into a dispersionless mode with a single velocity and a single deformation potential [7]. Historically, TA modes have been neglected because their matrix element is zero for intravalley scattering within a band located at the center of the Brillouin zone [13].

This isn't the case for silicon, hence in a more comprehensive approach (where scattering with *all* phonon modes matters) intravalley scattering with TA modes should be considered. Unlike the traditional approach, this work considers scattering with LA and TA modes separately [4]. Each phonon dispersion branch from Figure 5 (including the optical modes) is treated with the isotropic approximation

$$\omega_q = \omega_0 + v_s \, \mathrm{q} + \mathrm{c}q^2 \qquad (1)$$

where ω_q is the phonon frequency and q the wave vector. For the acoustic phonons, the parameters *vs*and *c* can be chosen to capture the slope of the dispersion near the Brillouin zone center and the maximum frequency at the zone edge. The choice ofparameters for longitudinal optical (LO) phonons insures that they meet the zone edge LA frequency. For both TA and transverse optical (TO) phonons the zone edge slope, i.e. their group velocity is fit to zero. The continuous (longitudinal) and dashed (transverse) lines in Figure 5 represent these quadratic approximations, and the fitting coefficients. Quartic polynomials would offer a better fit in the <100>crystal direction but no advantage in the other directions, hence the quadratics are entirely sufficient for this isotropic approximation. They track the phonon dispersion data closely, especially in the regions relevant to electron-phonon scattering in silicon: near the Brillouin zone center for long wavelength intravalley acoustic phonons, and near the frequencies corresponding to intervalley f- and g-type phonons [4]. The quadratics are also easy to invert and, where needed, to extract the phonon wave vector as a function of frequency.

The same approach can be used to extend this phonon

dispersion model to other materials or confined dimensions. Changes in the phonon dispersion due to strain or confinement (e.g. in nanostructures) can be easily included. The challenge in this case lies chiefly in determining the correct modified phonon dispersion to use in such circumstances [3].

The electron-phonon scattering rates need to be numerically recomputed with the modified phonon description (as outlined below), which can be done efficiently if the dispersion is written as a set of analytic functions, like the polynomials in this work.

2. Physical Models

Numerical simulations are performed by self-consistently solving the 2-D Schrodinger and Poisson equations in the coherent transport regime in the presence of fixed charge centers trapped at the SiO_2/high-κdielectric interface.

In order to reduce the numerical burden the coupled mode space (CMS) approach is used within the NEGF formalism [4]. According to the CMS approach the discrete electron correlation function reads:

$$G^<(i_1,i_2,j_1,j_2,k_1,k_2,E) = \sum_{n,m} G^<_{m_s}(i_1,i_2,n,m,E)\,\Phi^n_{i_1}(j_1,k_1)\Phi^{m^*}_{i_2}(j_2,k_2) \quad (2)$$

where $\{\Phi^n_i\}_{n=1,2,\ldots,N_yN_z}$ is the orthonormal set of eigen-functions solution of the 2-D Schrodinger problem for the i^{th} slice of the device, $G^<_{m_s}$ is the mode-space counter part of the real-space Green's function and Ny(Nz) indicates the number of discretization nodes along the y(z) confinement direction. The solution in the transverse plane is obtained assuming close boundary conditions with vanishing wave functions at the gateoxide interface [11]. The Green's functions in the mode space are obtained as solution of the two of kinetic equations

$$\left[E - H_{m_s} - \sum_{m_s}\right]G_{m_s} = I \quad (3)$$

$$G^<_{m_s} = G_{m_s}\sum\nolimits^<_{m_s} G^\dagger_{m_s}$$

where $\sum^<_{m_s}$ and $\sum_{m_s}$ are the lesser-than and retarded self-energies describing the ideal infinite equipotential contacts, H_{m_s} is the mode-space Hamiltonian and I is the identity matrix, for every energy E, and then evaluating the real space electron density through the integral:

$$n_{i,j,k} = \frac{-ig_vg_s}{\Delta x}\int\frac{dE}{2\pi}G^<(\mathrm{i,i,j,j,k,k},E) \quad (4)$$

Where g_{vs} are the valley and spin degeneration coefficients, respectively [9].

The Poisson equation

$$\nabla\big(\varepsilon(r)\nabla\phi(r)\big) = \rho(r) \quad (5)$$

is solved in the 3-D domain using the box-integration method, where $\varepsilon(r)$ is the position dependent dielectric constant, $\rho(r)$ is total charge density accounting for both electrons and fixed charges, and $\phi(r)$ is the self-consistent electrostatic potential.

3. Electron-Phonon Scattering

Scattering by lattice vibrations (phonons) is one of the most important processes in the transport of carriers through a semiconductor. It is this scattering that limits the velocity of electrons in the applied electric field, and from this point of view transport can be seen as the balance between accelerative forces (the electric field) and dissipative forces (the scattering). The treatment of electron-phonon scattering in NEGF simulations is based on the assumption that lattice vibrations cause small shifts in the energy bands, and this additional potential *U* causes the scattering process, with the matrix element

$$M(k,k') = \langle k'|U|k\rangle \quad (6)$$

between the initial state k and the final state k'. This matrix element contains the momentum conservation condition, k' = k ± q + G, where q is the phonon wave vector, G is a reciprocal lattice vector, and the upper and lower signs correspond to the absorption and emission of a phonon. The electronic wave functions are typically taken to be Bloch functions that exhibit the periodicity of the lattice. The electron-phonon scattering rate is based on Fermi's Golden Rule, which is derived from first-order time-dependent perturbation theory and gives the transition probability between the two eigenstates

$$P(k,k') = \tfrac{2\pi}{\hbar}|M(k,k')|^2\delta\big(E_k - E_{k'} \pm \hbar\omega_q\big) \quad (7)$$

where the upper and lower signs have the same meaning as in the previous paragraph. It is assumed that the scattering potential is weak, such that it can be treated as a perturbation of the well-defined energy bands, and the *δ*-function ensures that two collisions do not "overlap" in space or in time, i.e. they are infrequent, or that the scattering time is much shorter than the time between collisions. The total scattering rate out of state k is obtained by integrating over all final states k*0* the electron can scatter into. Mathematically, this integration can be carried out over k*0* or q with the same result. In those cases in which the matrix element is independent of the phonon wave vector, the matrix element can be removed from the integral, which leaves a total scattering rate directly dependent on the density of states:

$$\Gamma(k) = \tfrac{2\pi}{\hbar}|M(k)|^2 g_d\big(E_k \pm \hbar\omega_q\big) \quad (8)$$

where *M*(k) includes the dependence on the phonon occupation of states, on the wave function overlap integral and on the deformation potential characteristic of the particular phonon involved. 1 The dependence of the total scattering rate on the density of final states has a satisfying interpretation, as it gives us a means for comparing scattering rates in 1-, 2- or 3-dimensional systems. In three dimensions the electron-phonon scattering rate increases roughly as the

square root of the electron energy, just like the density of states

$$g_d(E_k) = \frac{(2m_d)^{3/2}}{2\pi^2\hbar^3}\sqrt{E_k(1+\alpha E_k)}(1+2\alpha E_k) \qquad (9)$$

written here in the non-parabolic, analytic band approximation adopted in this work, where $m_d = (m^2 t\, ml)^{1/3}$ is the electron density of states effective mass.

4. Discussions

Rapid device scaling pushes the dimensions of the field effect transistors to the nanometer regime. In this regime of operation quantum effects play an important role in determining the transistor characteristics. These effects can be accurately predicted only using quantum mechanical based device simulation. Non-equilibrium Green's function formalism (NEGF) provides a rigorous description of quantum transport in nanoscale devices. Computational efficiency is needed to make the device simulation suitable for device design and characteristic prediction. The NEGF method, unfortunately, has the disadvantage of being heavy in computations. The Real-space (RS) representation is the most accurate yet complex representation used in the NEGF. The geometry of fully-depleted double gate (DG) MOSFETs, however, permits the use of a simpler representation, the mode-space (MS) which is computationally efficient.

Electrostatic and carrier transport problems are coupled together. To determine the electrostatic potential by Poisson's equation, we need the carrier distribution. At the same time, the carrier distribution is obtained from transport equations which depend on the electrostatic potential. The solution of the NEGF and Poisson's equation is carried out by the self-consistent field method. It is an iterative method starts by assuming an initial guess for the potential distribution in the device. According to this potential, the NEGF is used to calculate the electron and hole concentrations in the device. With the electron and hole concentrations are known, Poisson's equation can be solved yielding a new potential distribution. The new potential is compared to the old potential and the solution cycle isrepeated until self consistent solution for the potential is obtained. Self-consistency criterion is that the difference in potential between two successive iterations drops below a certain tolerance.

In mesoscopic devices electrons may transport from one side of the device to the other side with little or no scattering at all. In this case, the phase of the electrons wave nature plays an important role in the transport process because electrons can interfere instructively or destructively. Thus, we can't describe the transport without including the wave nature of the electrons.

Figure 4 depicts the electron density along the channel of a DG MOSFET calculated by both the semi-classical BTE and the Schrödinger equation. Due to the interference between the incident and reflected electron waves, carrier density oscillations can be seen near the channel barrier edges. At room temperatures, the interference effect is somewhat washed out by the statistics. At low temperatures, however, the oscillation patterns become sharper, indicating strong interference. In this new algorithm, the NEGF simulations do not show any such effect a two-dimensional analytical model for graded channel dual material double gate field effect transistor with oxidespacer has been developed. The potential distribution under oxide spacer regions has been formulated by using conformal mapping technique to consider fringing field effect. The potential profile for channel region has been calculated by solving two-dimensional Poisson's equation and 2-D Schrödinger equation as show in Figure 2.

5. Results

In Figure 2 shows the plot of potential at T=300 K for SI nanowire (D = 3 nm, L = 10 nm) placed on SiO_2 dielectric layer of thickness tox = 1.0 nm at a back-gate voltage of 0 V and a surface donor density of 1×10^{20} cm^{-3}. The color scale shows the potential distribution in the nanowire as well as the substrate. The inset on the right is a plot of potential profile in a cross-sectional plane of the nanowire in the middle of the FET channel, indicating the Y distribution of potential with the inset color scale.

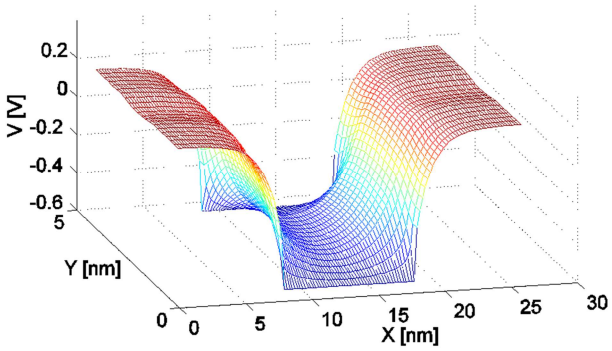

Figure 2. *Simulated constant potential 2D mesh of channel nMOSFET. The contours are labeled by their band bending w.r.t neutral ni-type regions. The drain is biased at 0.001 V and the gate voltage is slightly below the threshold.*

In this section we describe how one can reach the NEGF equations startingfrom the wave-function approach described in the previous section.

This isn't a formal derivation of the non-equilibrium Green's function formalism.

For double gate transistor, the device is fully depleted below threshold voltage, V_{TH}.

As gate voltage is increased, the electron concentration in the channel increases. At threshold voltage, peak electron concentration, n, becomes equal to the doping concentration, N_D. Above threshold voltage, the diameter of this region, where $n=N_D$, increases as the gate voltage increases.

At flat-band voltage, V_{FB}, he entire cross section of the device becomes neutral. Thus, Double gate transistor follows volume conduction mechanism whereas inversion-mode

MOSFET follows surface conduction mechanism.

Above flat-band voltage, charge carriers are accumulated under oxide-semiconductor interface which is not desirable because it causes surface phonon scattering and also reduces the mobility of the carriers and hence the maximum output current.

The electron concentration contour plots for these different states are shown in Figure 3.

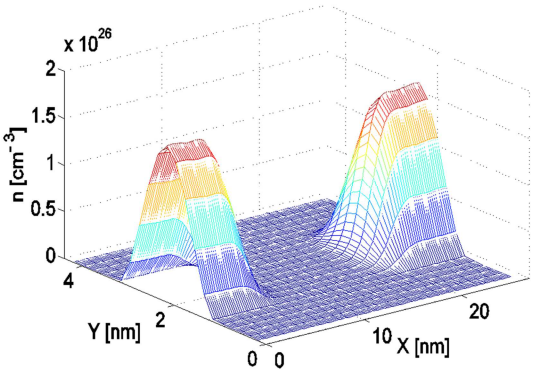

Figure 3. *The total 3D electron density, n(x,y), in the on-state. The thin silicon body is volume inverted, and the electron density goes to zero at the top and bottom oxide/silicon interface (1.0nm). Quantum effects due to confinement are accurately captured by n.*

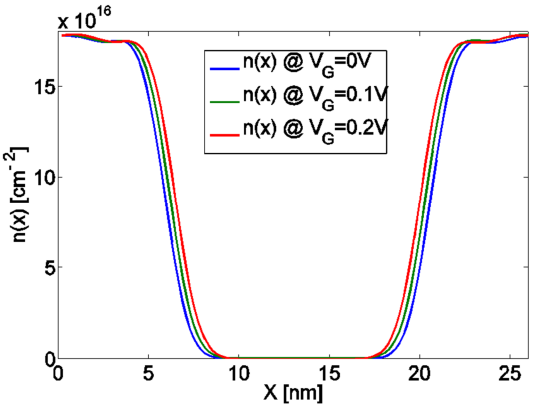

Figure 4. *The electron density along the channel of a DG-SOI MOSFET calculated by both the quantum transport model for different value of VG.*

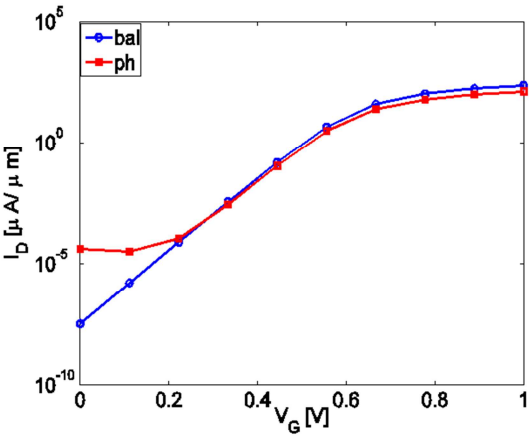

Figure 5. *The I_{DS} vs. V_{GS} characteristics for the model device from both the quantum (blue line) and phonon effect (red line) ballistic transport models. The ballistic off-current is higher from the quantum model due to source-to-channel tunneling.*

Figure 5 shows drain current vs. gate voltage characteristic curves for inversion-mode MOSFET (N+NiN+). For inversion-mode MOSFET, below flat-band voltage, V_{FB}, the body is Ni-type neutral and the device is in off-state. As the gate voltage is increased, the intrinsic are pushed away from oxide-semiconductor interface and a negative space charge region or depletion region is created. Thus, above flat-band voltage and below threshold voltage, V_{TH}, the body is fully or partially depleted and the device is off. Above threshold voltage, more negative charges are accumulated, an n-type layer is formed, a channel is created between source and drain and the device becomes turned on.

In Figure 6, Figure 7, Figure 8 There is no presence for the coupling term below the subband energy. This is identified by the blue region below the solid line.

This happens simply because there are no states at this region. Above the subband energy, there is an observed oscillation in the coupling terms versus the longitudinal energy and the position along the x -direction. These oscillations are identified in the graph by the alternation of bright and dark regions. We relate this oscillation to the well known quantum interference effect.

Interference occurs between the electron waves incident and reflected from the energy barrier; the reflected wave interferes constructively or destructively with the incident wave. At high temperature, the quantum interference effect may not be observed in the electron density because it is washed out by the statistics, however, it can be observed at low temperature.

The quantum interference effect can be observed in the local density of states (LDOS) before applying the statistics. For example, the 1st mode 2D LDOS at *Tsi*=3nm in the off-state is shown in Figures 6, 7, 8. The interference pattern is clear especially for the drain region. In that region, the energy barrier is relatively large and most of the incident wave from the drain contact is reflected blue.

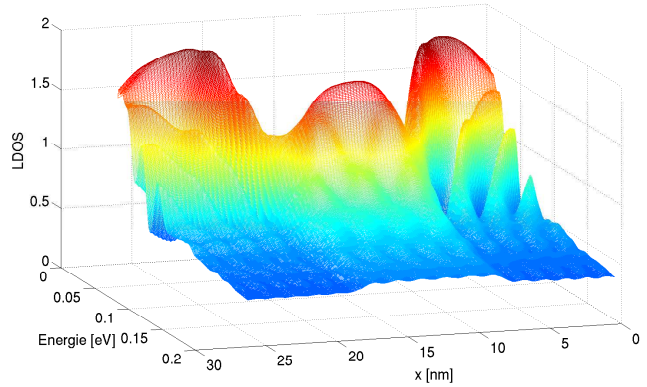

Figure 6. *The 1st mode 2D LDOS as a function of Energieand x at T Si = 3 nmin the off-state. The scale on the right side of the graph gives the value of the coupling term versus the intensity where brighter regions mean larger value of the coupling term.*

It is seen that the coupling effect between the two modes has larger values above the top of the energy barrier compared with the rest of the device.

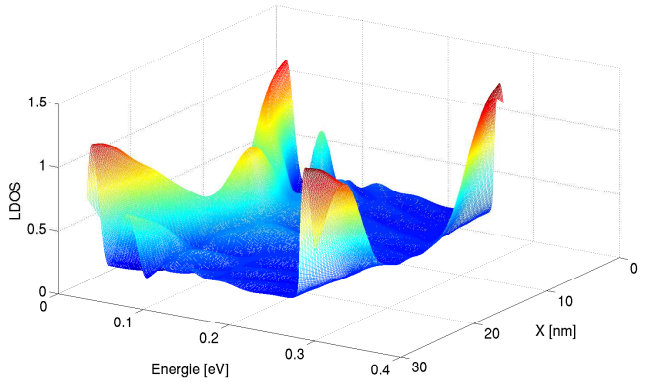

Figure 7. *The 2nd mode 2D LDOS as a function of Energieand x at T Si = 3 nm in the off-state. The scale on the right side of the graph gives the value of the coupling term versus the intensity where brighter regions meanlarger value of the coupling term.*

Also some oscillations can be identified where dark and bright regions alternate. These oscillations are quantum interference effect. However, it is difficult to explain the oscillation pattern because it is generated from the interaction of two modes, and not from a single mode with itself as in Figures 6, 7, 8. A similar behavior was obtained for the higher order coupling terms.

The threshold voltage of a DG MOSFET is defined as the gate voltage when the electron densities in the front or the back channel, formed near front or back Si/SiO_2 interfaces, respectively, equals the doping density of the channel.

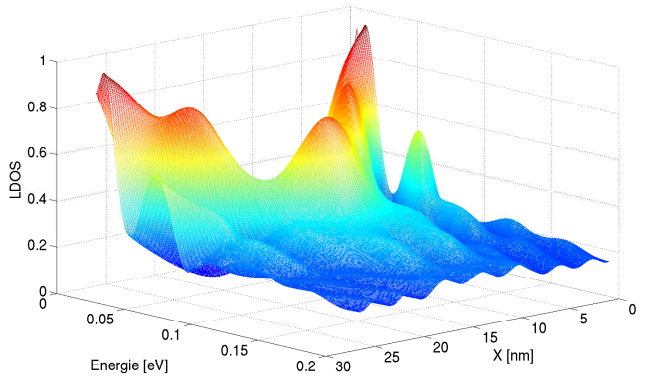

Figure 8. *The 3rd mode 2D LDOS as a function of Energieand x at T Si = 3nmin the off-state. The scale on the right side of the graph gives the value of the coupling term versus the intensity where brighter regions meanlarger value of the coupling term.*

It should be noted that the minima of front or back surface potential determines the threshold voltage of DG MOSFET.

Moreover, the conventional way of using the surface band bending equal to 2qIB, where IB=ln(NA/ni)kT/q, to define the thresholdcondition becomes irrelevant. An alternative is to define the threshold voltage as the gate voltage at which the sheet density of inversion carriers reaches a value of QTH adequate to identify the turn-on condition. Such a definition is equivalent to the constant-current V_{TH} simulate widely used both in experiments and simulations.

Figure 9 shows the variation of threshold voltage for silicon-film thicknesses (tsi) of 3 nm and SiO_2 layer thickness (tox) of 1 nm, with the effective channel length ranging from technology nodes 10 nm.

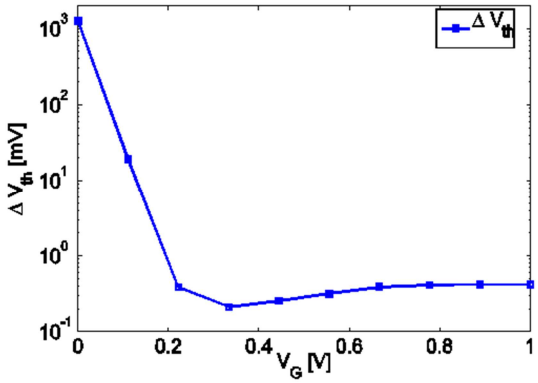

Figure 9. *Plot of calculated threshold voltage and threshold sensitivity to body thickness variation as a function of the gate voltage.*

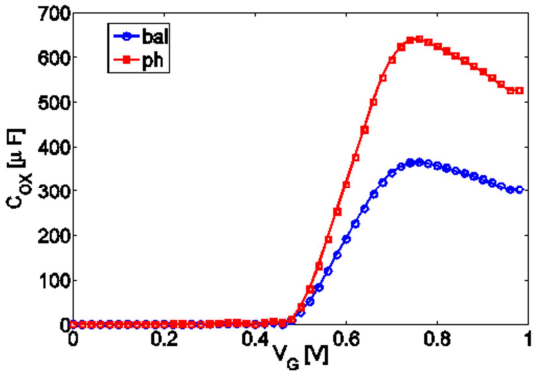

Figure 10. *Typical as-simulate split C-V_G characteristics for double gate DG MOSFET with 10nm length channel SiO_2/1nm double gate stack for ballistic (blue line) and phonon (red line).*

Simulation results of double gate MOSFET for gate capacitance (GC) at different gate voltages and oxide thickness at a constant drain voltage of 10mV is shown in Figure 10. It can be observed from the Figure that in double gate MOSFET as theoxide thickness goes down from 1.5 nm to 0.7 nm the quantum capacitance (QC) increases significantly as the gatevoltage increases from 0.5 V and above. This increment in quantum capacitance is observed up to a gate voltage of 10 mV.

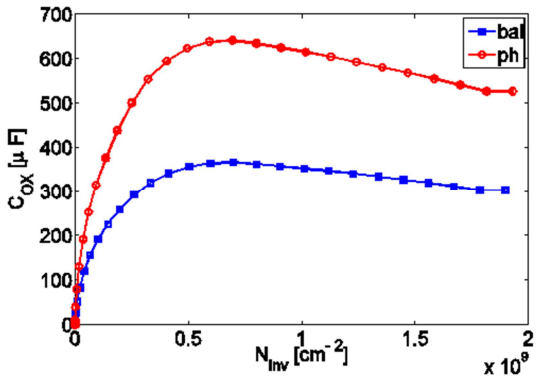

Figure 11. *Typical as-simulate split C-Ninv characteristics for double gate DG MOSFET with 10nm length channel SiO_2/1nm double gate stack for ballistic (blue line) and phonon (red line).*

Figure 11 shows the Ninv representation of quantum capacitance against gate voltage. It can also be observed from the simulation that at a very low gate voltage such as at 0 V and 1.0 V the value of quantum capacitance is same for all oxide thicknesses considered here.

6. Conclusion

Recent analysis has shown a strong correlation between intrinsic transistor delay, source injection velocity, and low-field carrier mobility.

In addition, the band structure of silicon results in low transport effective mass and high inversion charge density for electrons on (100)-oriented substrates. As a result, two different Green's functions exist, the retarded and the advanced Green's function.

The electrical characteristics and intrinsic performance of double gate nanowire MOSFETs, simulated using a CMOS compatible top-down approach, were investigated in this paper. The double gate device architecture benefits from excellent gate control, cut-off behavior and immunity to short channel effects compared to planar MOSFETs. However, degraded transport is often observed for both types of carriers due to non-ideal sidewalls with phonon. To overcome this problem, two types of process-based performance boosters, applicable on suspended Si nanowires, were developed in this paper: a novel uniaxial strain engineering method for n-MOSFETs and hydrogen thermal annealing process for ni-MOSFETs. The impact of these performance boosters on the transport properties of double gate nanowire MOSFETs with various channel dimensions were studied in detail.

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